TELEDYNE | Teledyne e2v

CCD201-20

1MP BSI EMCCD

KEY FEATURES

- 1024 x 1024 active pixels
- 13µm square pixels
- Single photon sensitive
- Variable multiplication gain
- Additional conventional output amplifier
- Frame Transfer
- Inverted mode operation for low dark current
- 36-pin ceramic package

TYPICAL APPLICATIONS

- Advanced Microscopy
- Fast Astronomy
- Quantum Imaging

PART REFERENCES

Please see last page for full list of available parts.

GENERAL DATA

Format	
Image Area	13.3 × 13.3 mm
Active Pixels	1024 x 1024 (note 1)
Pixel Size	13 × 13 µm
Number of output amplifiers	2 (Electron multiplying and Conventional)
Package	
Package size	37.4 mm × 26.5 mm
Number of pins	36
Window Material	Removable Glass
Performance	
Typical amplifier responsivity	5.3 µV/e^- (OSH) 1.4 µV/e^- (OSL)
Typical readout noise	<1e^- at 1MHz at 1000x Gain 3.1e^- at 50kHz using OSH amp
Max output data rate	20 MHz
Typical pixel charge capacity	80 ke^-/pixel
Typical dark signal (20°C)	260 e^-/pixel/s

OVERVIEW

The CCD201-20 is a frame transfer, electron multiplying CCD sensor designed for extreme performance in high frame rate, ultra-low light applications. The Teledyne e2v back-thinning process ensures high quantum efficiency over a wide range of wavelengths.

An electron multiplying CCD functions by having an extended readout register with variable gain from 1x to 1000x prior to voltage conversion in the output amplifier. This allows readout noise to be effectively eliminated while maintaining fast readout rates.

The device can also be read out without using the gain register via the High Responsivity Output amplifier (OSH) for high dynamic range.

Teledyne UK Limited, Waterhouse Lane, Chelmsford, Essex CM1 2QU United Kingdom Teledyne UK Ltd. is a Teledyne Technologies company.
Telephone: +44 (0)1245 493493   Facsimile: +44 (0)1245 492492
Contact Teledyne e2v online at www.teledynespaceimaging.com/en-us/contact-us

PERFORMANCE

Except where otherwise specified, the following are measured at 18°C at a pixel rate of 15 MHz, with typical operating voltages. For the S29 variant, the parameters relating to the OSH amplifier do not apply; all other parameters are unchanged.

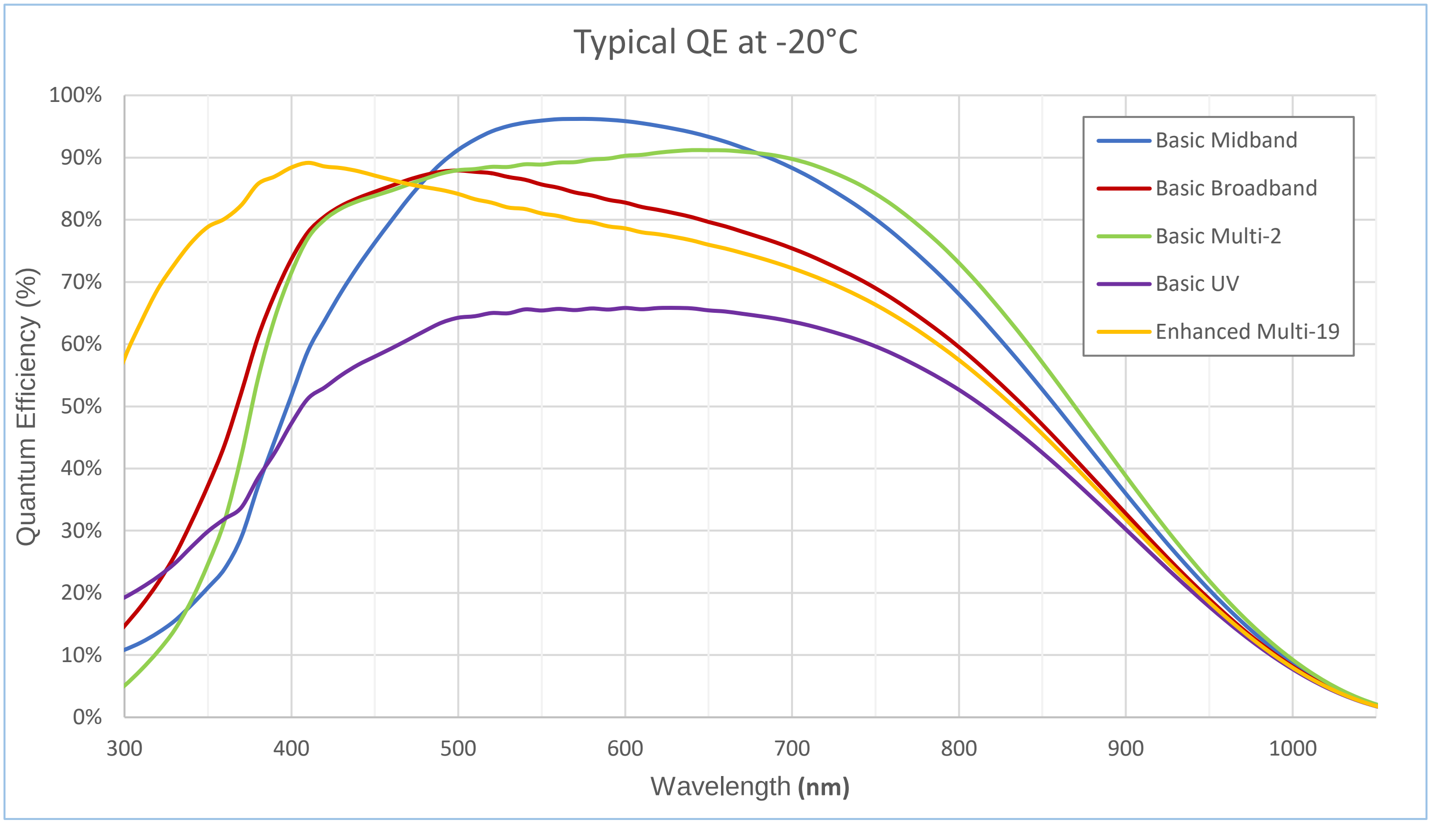
Parameter	Min	Typical	Max	Units	Note
Output amplifier responsivity, OSH amplifier	-	5.3	-	µV/e^-	2
Output amplifier responsivity, OSL amplifier	-	1.4	-	µV/e^-	3
Multiplication register gain, OSL amplifier	1	-	1000		4
Peak signal - 2-phase IMO	65k	80k	-	e^-/pixel	5
Charge handling capacity of multiplication register	-	730k	-	e^-/pixel	6
Charge handling capacity of OSH amplifier	-	280k	-	e^-	7
Charge handling capacity of OSL amplifier	-	1M	-	e^-	7
Readout noise at 50 kHz with CDS, OSH amplifier	-	3.1	-	e^- rms	7
Readout noise at 1 MHz with CDS, OSH amplifier	-	6.0	-	e^- rms	7
Amplifier reset noise (without CDS), OSH amplifier	-	50	-	e^- rms	7
Readout noise at 15 MHz with CDS, OSL amplifier	-	43	-	e^- rms	3, 7
Amplifier reset noise (without CDS), OSL amplifier	-	100	-	e^- rms	3, 7
Readout noise at 1 MHz (1000x gain)	-	<1	-	e^- rms	7
Maximum frequency (settling to 1%), OSH amplifier	-	-	3	MHz	7,8
Maximum frequency (settling to 5%), OSH amplifier	-	-	4.5	MHz	7,8
Maximum frequency (settling to 1%), OSL amplifier	-	-	13	MHz	7,8
Maximum frequency (settling to 5%), OSL amplifier	-	-	20	MHz	7,8
Maximum parallel transfer frequency	-	0.9	-	MHz	2
Dark signal equivalent at 20°C	-	260	530	e^-/pixel/s	9, 10
Dark signal non-uniformity (DSNU) equivalent at 20°C	-	90	-	e^-/pixel/s	11
Excess noise factor	-	$\sqrt{2}$	-		12

NOTES

1. For the Multi-19 variant a reduced format of 1018 x 1018 is recommended due to reduced responsivity at the edges of the image area.
2. Measured at a pixel rate of 1MHz.
3. No EM gain applied.
4. Some increase of RØ2HV may be required throughout life to maintain gain performance.
5. For Multi-2 and Multi-19 variants, the peak signal is 55k e^- typical and 40k e^- min.
6. When multiplication gain is used, a linear response is achieved for output signals up to 400 ke^-.
7. These values are inferred by design and not measured.
8. The quoted maximum frequencies assume a 20 pF load and correlated double sampling (CDS) are being implemented. If instead a single sampling is used, the output will be settled to 1% at 20 MHz typically.
9. The quoted dark signal has the usual temperature dependence for inverted mode operation. For operation at high frame rates with short integration times, there will also be a component generated during readout through the register.

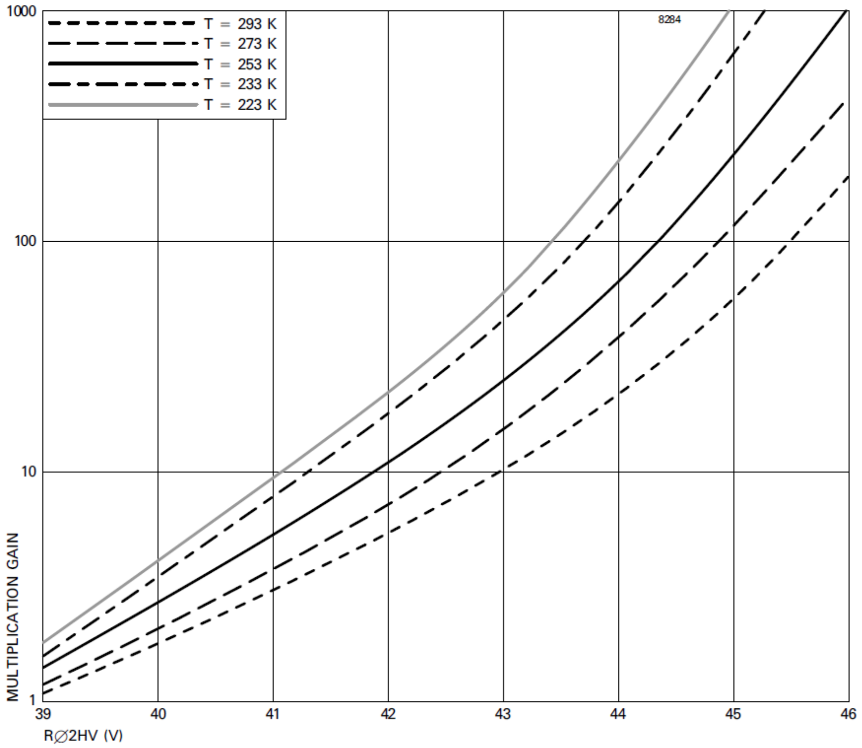
   There exists a further weakly temperature dependent component, the clock induced charge (CIC), which is independent of the integration time. For more information, refer to the technical note "Dark Signal and Clock-Induced Charge in L3Vision™ CCD Sensors".
10. For fringe suppression variants, the dark signal will be higher (typical and maximum are 400 and 600 e^-/pixel/s respectively).
11. DSNU is defined as the 1σ variation of the dark signal.
12. The excess noise factor is defined as the factor by which the multiplication process increases the shot noise on the image when multiplication gain is used.

SPECTRAL RESPONSE



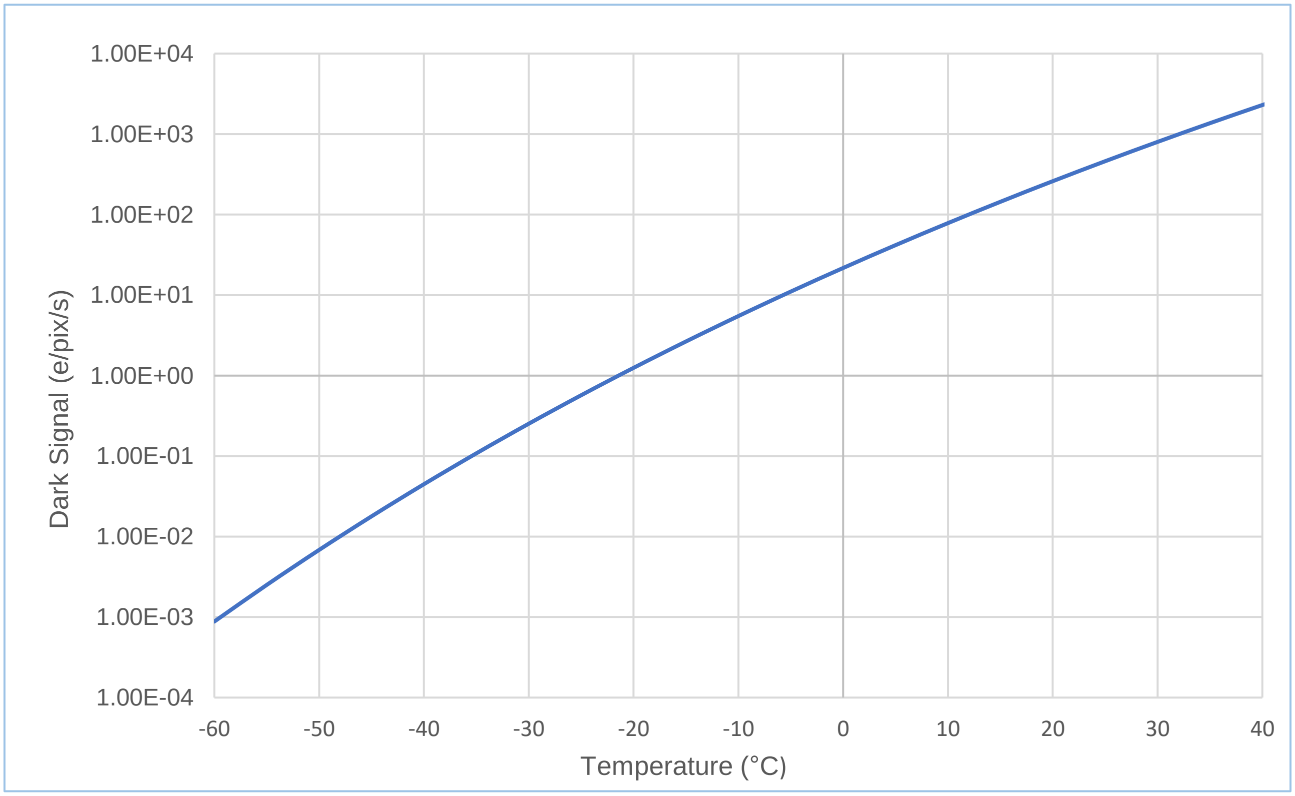
Devices can be supplied with alternative anti-reflection coatings optimised for different wavelengths – details from Teledyne e2v.

TYPICAL VARIATION OF MULTIPLICATION GAIN WITH RØ2HV



TYPICAL VARIATION OF IMO DARK SIGNAL WITH TEMPERATURE (not measured)

Dark signal is a strong function of temperature and the typical average (background) dark signal at any temperature T (kelvin) between 150 K and 300 K is given by $Q_d/Q_{do} = 1.14 \times 10^6 T^3 e^{-9080/T}$ where Q_{do} is the dark current at 293K.



COSMETIC SPECIFICATION

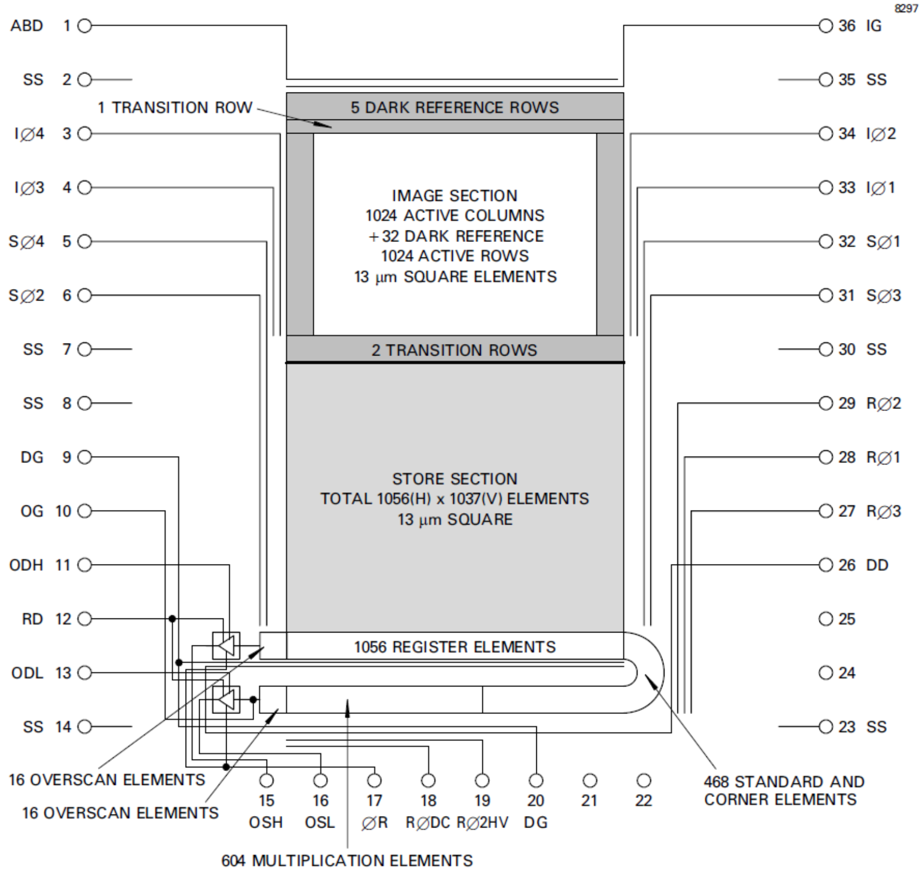
All cosmetic tests are performed at 18 ± 3ºC in 2-phase inverted mode with a readout rate of 15MHz.

Grade	0	1
White Defects	10	24
White Columns	0	0
Black/Pin-head Columns	0	1

Cosmetic definitions

White Defects	White defects are pixels having a dark signal generation rate corresponding to an output signal of greater than 5 times the maximum dark signal level.
White Columns	A white column contains at least 9 white defects.
Black/Pin-head Columns	Black defects are counted when they have a responsivity of less than 80% of the local mean signal at approximately the specified gain and level of illumination. A black column contains at least 9 black defects. Pin-head columns are manifest as a partial dark column with a bright pixel showing photo-response at the end of the column nearest to the readout register. Pin-head columns are counted when the black column has a responsivity of less than 80% of the local mean signal at approximately the specified multiplication gain and level of illumination. A pin-head column contains at least 9 black defects.

DEVICE ARCHITECTURE



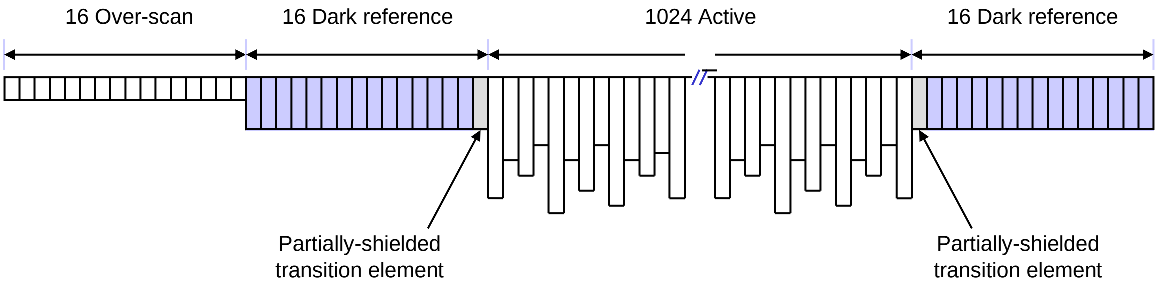
The rows and colums immediately adjacent to the active image area may be only partially shielded, i.e. transition elements, and should not be used for reference purposes.

The electrodes of the image and store sections are configured for four-phase clocking, but adjacent phases need to be joined off chip to run in two phase operation.

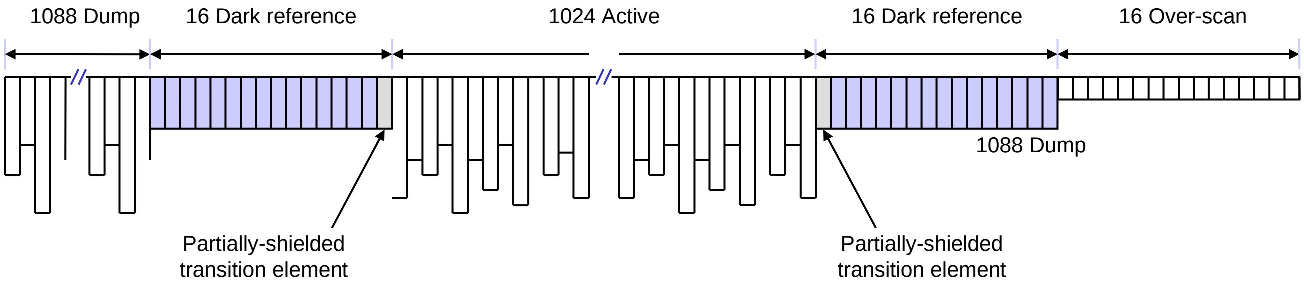
The multiplication register requires two extra drive phases, RØDC and RØ2HV.

There is a dump drain DD below the 1056 register elements adjacent to the store section with the charge dumping operation controlled by the dump gate DG.

LINE OUTPUT FORMAT (OSH AMPLIFIER)



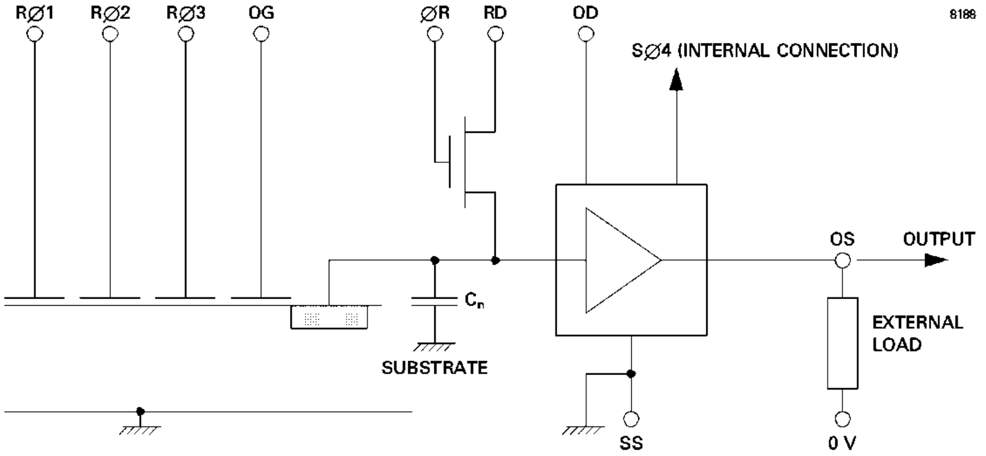
LINE OUTPUT FORMAT (OSL AMPLIFIER)



NOTES

13. There is a 1-line propagation delay between transferring a line from the store section to the standard register and reading it out through the OSL output amplifier.

OUTPUT CIRCUIT



The amplifiers have a DC restoration circuit that is internally activated whenever S∅4 is high.

Nominal Design Features (Not measured)

Feature	OSH	OSL
Output	OSH (pin 15)	OSL (pin 16)
External load	5 kΩ or 5 mA	3.3 kΩ or 7.5 mA
Output impedance	400 Ω	350 Ω
On-chip dissipation	30 mW	50 mW

CONNECTIONS TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

The table below gives the pin connections, functions and maximum ratings with respect to the substrate (SS).

Pin	Ref	Function	MIN (V)	MAX (V)
1	ABD	Anti-blooming drain (note 14)	-0.3	+25
2	SS	Substrate	0	
3	IØ4	Image Clock 4	-20	+20
4	IØ3	Image Clock 3	-20	+20
5	SØ4	Store Clock 4	-20	+20
6	SØ2	Store Clock 2	-20	+20
7	SS	Substrate	0	
8	SS	Substrate	0	
9	DG	Dump Gate	-20	+20
10	OG	Output Gate	-20	+20
11	ODH	Output Drain (OSH Amplifier)	-0.3	+32
12	RD	Reset Drain	-0.3	+25
13	ODL	Output Drain (OSL Amplifier)	-0.3	+32
14	SS	Substrate	0	
15	OSH	Output Source (OSH Amplifier) (note 15, 16)	-0.3	+25
16	OSL	Output Source (OSL Amplifier) (note 16)	-0.3	+25
17	ØR	Reset Pulse	-20	+20
18	RØDC	Multiplication Register DC Bias	-20	+20
19	RØ2HV	Multiplication Register Clock	-20	+50
20	DG	Dump Gate	-20	+20
21	n.c.	Not Connected	-	-
22	n.c.	Not Connected	-	-
23	SS	Substrate	0	
24	n.c.	Not Connected	-	-
25	n.c.	Not Connected	-	-
26	DD	Dump Drain	-0.3	+25
27	RØ3	Register Clock 3	-20	+20
28	RØ1	Register Clock 1	-20	+20
29	RØ2	Register Clock 2	-20	+20
30	SS	Substrate	0	
31	SØ3	Store Clock 3	-20	+20
32	SØ1	Store Clock 1	-20	+20
33	IØ1	Image Clock 1	-20	+20
34	IØ2	Image Clock 2	-20	+20
35	SS	Substrate	0	
36	IG	Isolation Gate	-20	+20

NOTES

14. The ABD pin is used for connection purposes and must be biased as specified even for non-anti-blooming variants.
15. OSH (pin 15) is not connected for the S29 variant.
16. Permanent damage may result if, in operation, OSL and OSH experience short-circuit conditions.

MAXIMUM VOLTAGE BETWEEN PAIRS

Pin	Ref	Pin	Ref	Min (V)	Max (V)
15	OSH	**11**	ODH	-15	+15
16	OSL	**13**	ODL	-15	+15
19	RØ2HV	**18**	RØDC	-20	+50
19	RØ2HV	**27**	RØ3	-20	+50
Output Transistor Current (mA)					20

OPERATING VOLTAGES

Typical operating voltages are as given in the table below. Some adjustment within the minimum-maximum range specified may be required to optimise performance.

Connection	Description	Phase Amplitude or DC Level (V)			Notes
		Min	Typical	Max	
IØ1, 2, 3, 4 high	Image section: clock high	+5	+7	+9	17
IØ1, 2, 3, 4 low	Image section: clock low	-6	-5	-4	
SØ1, 2, 3, 4 high	Store section: clock high	+5	+7	+9	17
SØ1, 2, 3, 4 low	Store section: clock low	-6	-5	-4	
RØ1, 2, 3 high	Register: clock high	+8	+12	+13	
RØ1, 2, 3 low	Register: clock low	-	0	-	
RØ2HV high	Register HV phase high	+20	+40	+50	4
RØHV low	Register HV phase low	0	+4	+5	
ØR high	Reset clock high	-	+10	-	18
ØR low	Reset clock low	-	0	-	
RØDC	Register DC phase	+2	+3	+5	
OG	Output gate voltage	+1	+3	+5	19
IG	Isolation gate voltage	-	-5	-	
SS	Substrate	0	+4.5	+7	20
ODL, ODH	Output drain	+25	+28	+32	
RD	Reset drain voltage	+15	+17	+20	19
ABD	Anti-blooming Drain	+10	+18	+20	
DG high	Dump gate high	-	0	-	
DG low	Dump gate low	+10	+12	+13	
DD	Dump drain	+20	+24	+25	

NOTES

17. IØ and SØ adjustment may be common. The high level may need to be adjusted to achieve correct charge transfer and the low level may need to be separately adjusted to achieve correct inverted mode operation that is uniform across the array.
18. ØRL and ØRH high level may be adjusted in common with RØ1, 2, 3.
19. Between the two amplifiers, common connections are made to the reset gates (ØR), reset drains (RD) and output gates (OG).
20. The SS voltage may also need to be adjusted to achieve correct inverted-mode operation.

ELECTRICAL INTERFACE CHARACTERISTICS

ELECTRODE CAPACITANCES AT MID CLOCK LEVELS					SERIES RESISTANCE	
Connection	**To SS**	**Inter-phase**	**Total**	**Units**	**Total**	**Units**
IØ1 + IØ2	7.8	4.8	12.6	nF	8	Ω
IØ3 + IØ4	7.8	4.8	12.6	nF	8	Ω
SØ1 + SØ2	7.8	4.8	12.6	nF	8	Ω
SØ3 + SØ4	7.8	4.8	12.6	nF	8	Ω
RØ1	68	98	166	pF	6	Ω
RØ2	56	68	124	pF	6	Ω
RØ3	89	74	163	pF	6	Ω
RØ2HV	15	18	33	pF	8	Ω

CLOCK TIMING REQUIREMENTS

The device is of a 4-phase construction, designed to operate in 2-phase inverted mode. This is achieved by applying common timings to phases ∅1 and ∅2, and phases ∅3 and ∅4 of the image and store sections. Suggested timing diagrams are shown in Figs. 8 - 13.

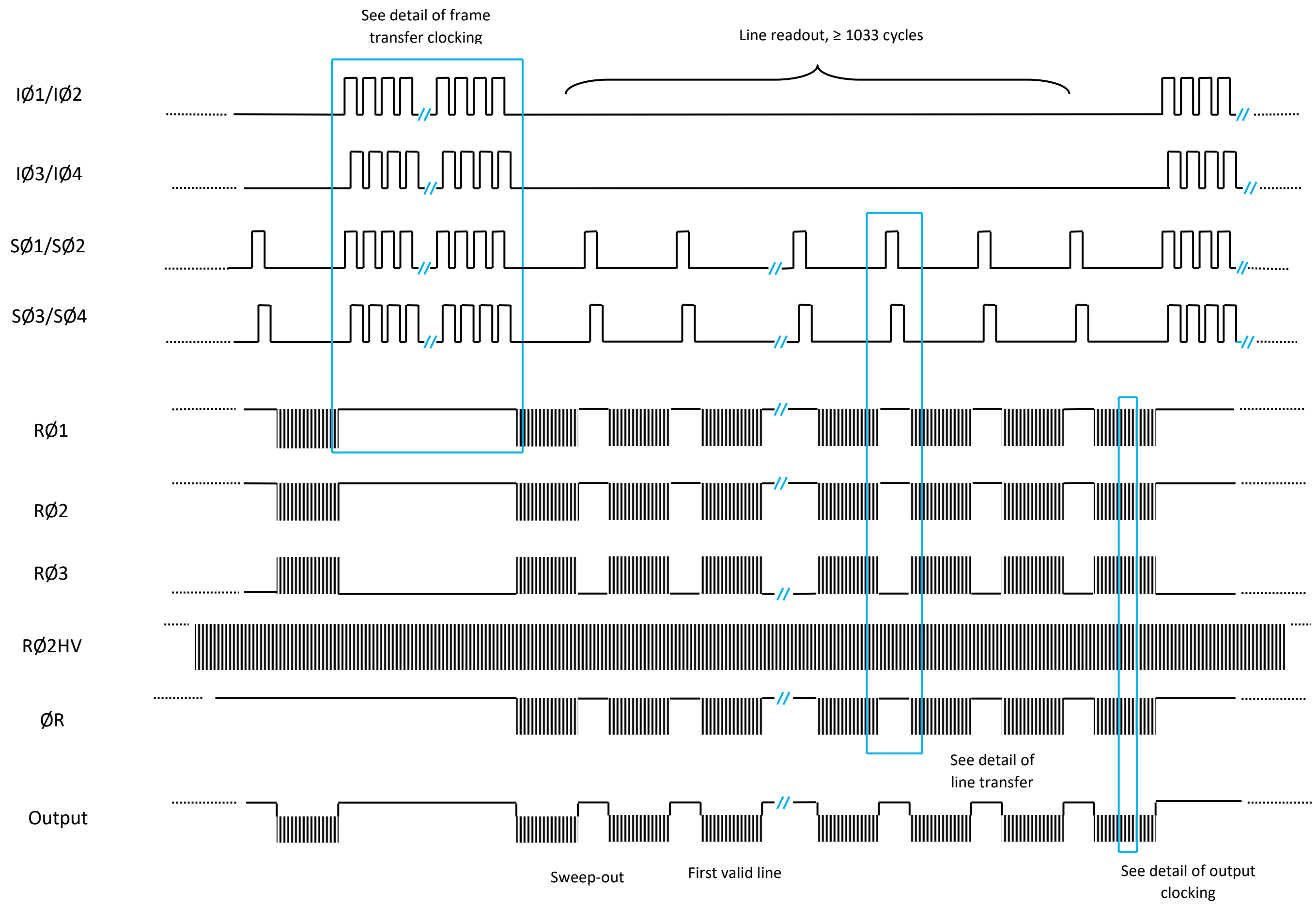
The following are suggested pulse rise and fall times.

Symbol	Description	Min	Typical	Max	Units	Notes
T_i	Line transfer time during FT	$2[t_{wi} - t_{oi}]$	1.5		µs	21, 22
t_{wi}	Image/store clock pulse width	$3t_{oi}$	1		µs	22
t_{oi}	Image/store clock pulse edge overlap	200	250		ns	22
t_{ri}	Image/store clock pulse rise time (10 - 90%)		50	$0.3\ t_{oi}$	ns	
t_{fi}	Image/store clock pulse fall time (10 - 90%)		50	$0.3\ t_{oi}$	ns	
t_{D1}	Image/store clock delay time at start of FT	20	40		µs	22
t_{D2}	Delay time, RØ stop to SØ rising	0.1	1		µs	22
t_{D3}	Delay time, SØ falling to RØ start	0.3	1		µs	22
t_{D4}	Delay time, RØ falling to DG falling	5	20		µs	22
t_{D5}	Delay time, DG falling to RØ rising	5	20		µs	22
T_{rr}	Register clock period		67		ns	21, 22
t_{w1}	Register pulse width, RØ1 (at 50% levels)		$T_{rr}/2$			22
t_{w2}	Register pulse width, RØ2 (at 50% levels)		$T_{rr}/4$			22
t_{w3}	Register pulse width, RØ3 (at 50% levels)		$T_{rr}/4$			22
t_{rr}	Register clock pulse rise time (10 - 90%)	5	10	$T_{rr}/5$	ns	
T_{fr}	Register clock pulse fall time (10 - 90%)	5	10	$T_{rr}/5$	ns	
t_{or}	Register clock pulse edge overlap (50% levels)	5	10	$T_{rr}/5$	ns	
t_{wx}	Reset pulse width (at 50% levels)	10	15	$T_{rr}/4$	ns	
t_{rx}	Reset pulse rise time (10 - 90%)	2	5	$T_{rr}/10$	ns	
t_{fx}	Reset pulse fall time (10 - 90%)	2	5	$T_{rr}/10$	ns	
t_{Dx}	Delay time, ØR falling to RØ2 falling (at 50%)	0	5	$t_{w2} - t_{wx}$	ns	

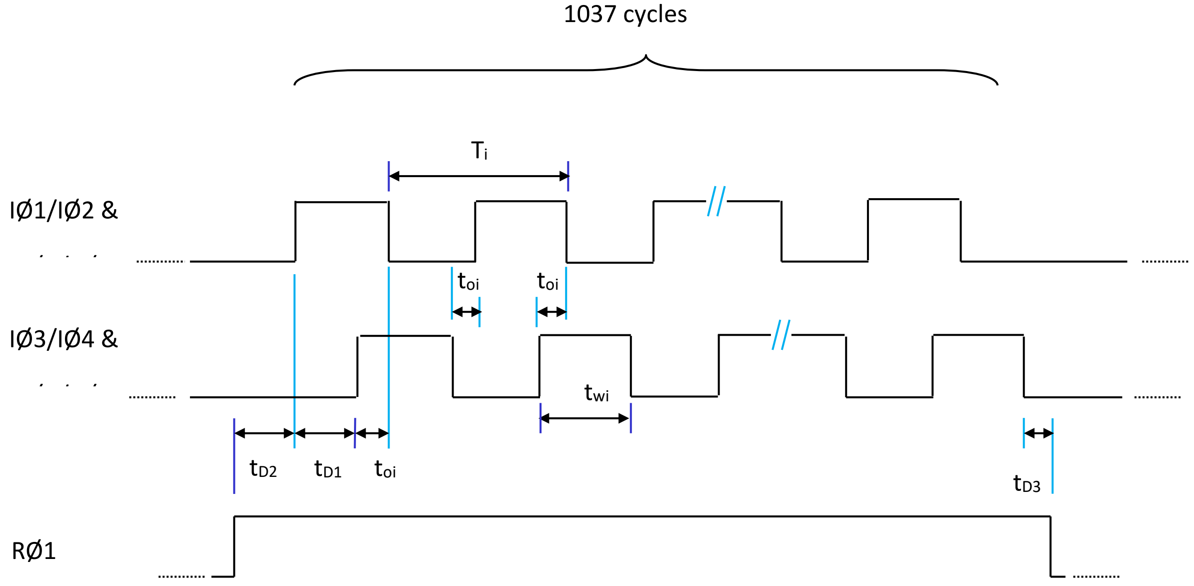
NOTES

21. As used for device testing at 15 MHz readout rate
22. No maximum other than set by system constraints.
23. Total line transfer time for line readout = tD2 + 2twi - toi + tD3

FRAME READOUT TIMING DIAGRAM

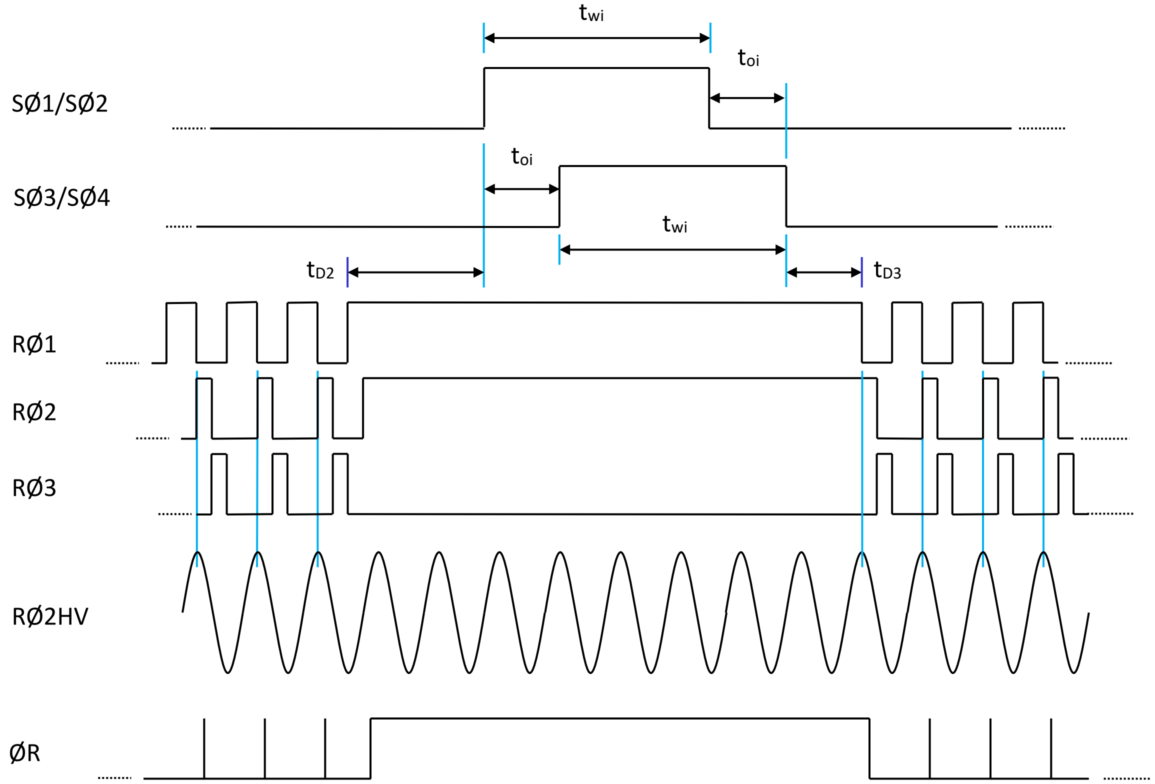


FRAME TRANSFER CLOCKING



DETAIL OF LINE TRANSFER

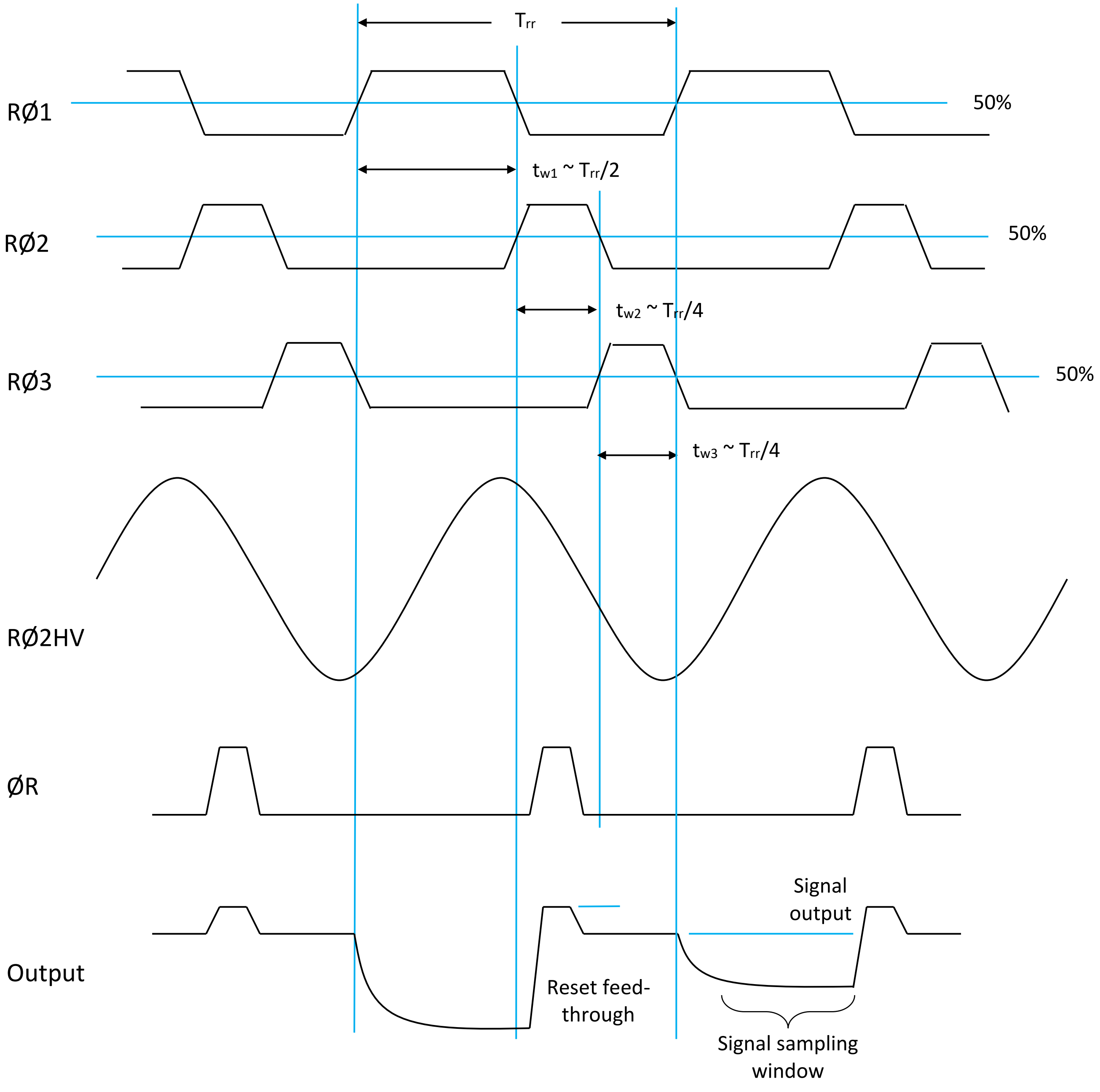
(Operation through OSL, see note 13 and note 24)



DETAIL OF OUTPUT CLOCKING

(Sinusoidal Clocking Scheme, see note 24, used for factory testing)

R∅2HV can also be of a trapezoidal pulse shape, as shown in Figure 12 overleaf. The RØ2HV pulse should reach full amplitude before R∅1 starts to fall. The edge times are not critical and could be ~5% of the read-out period.

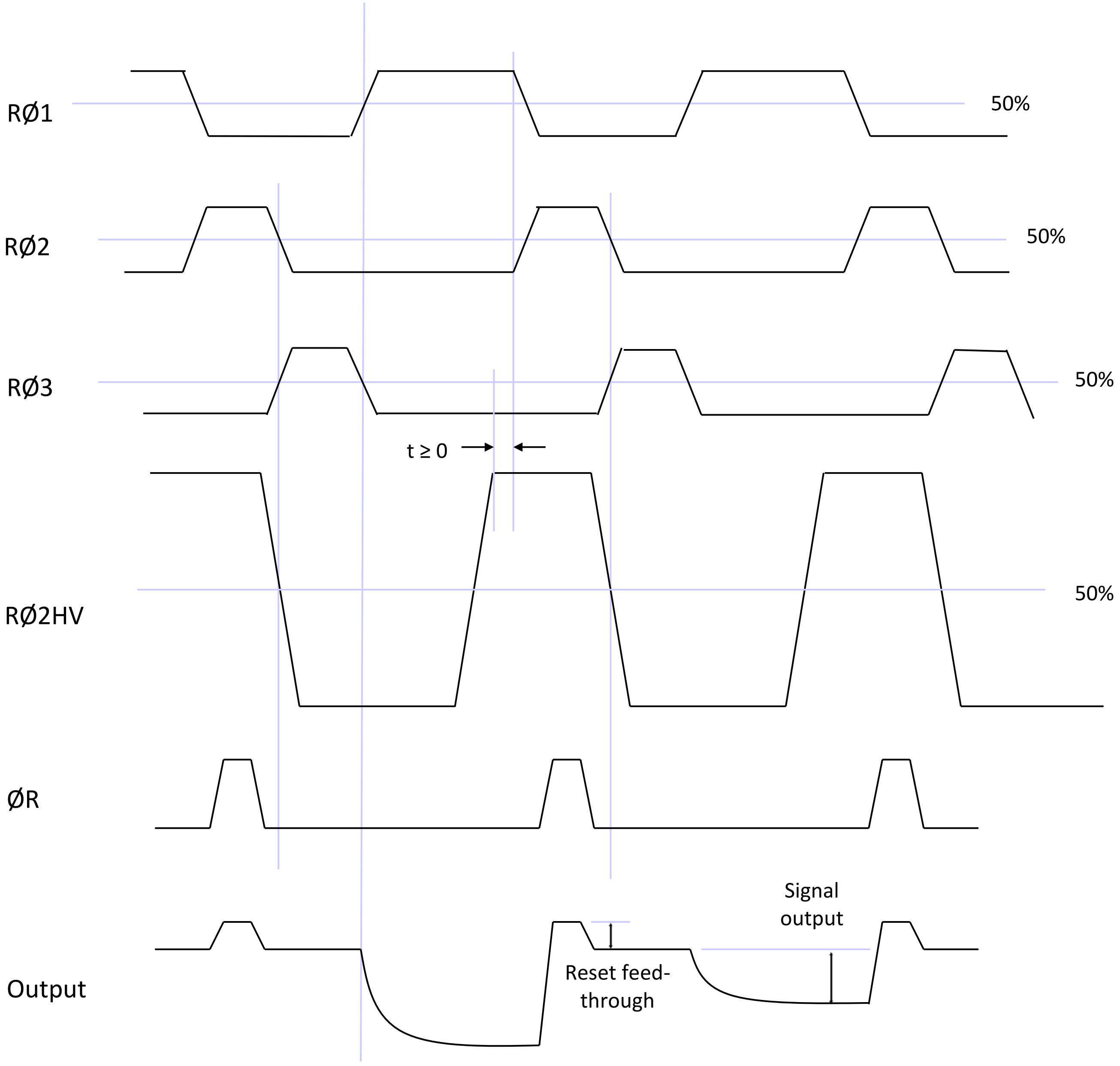


NOTES

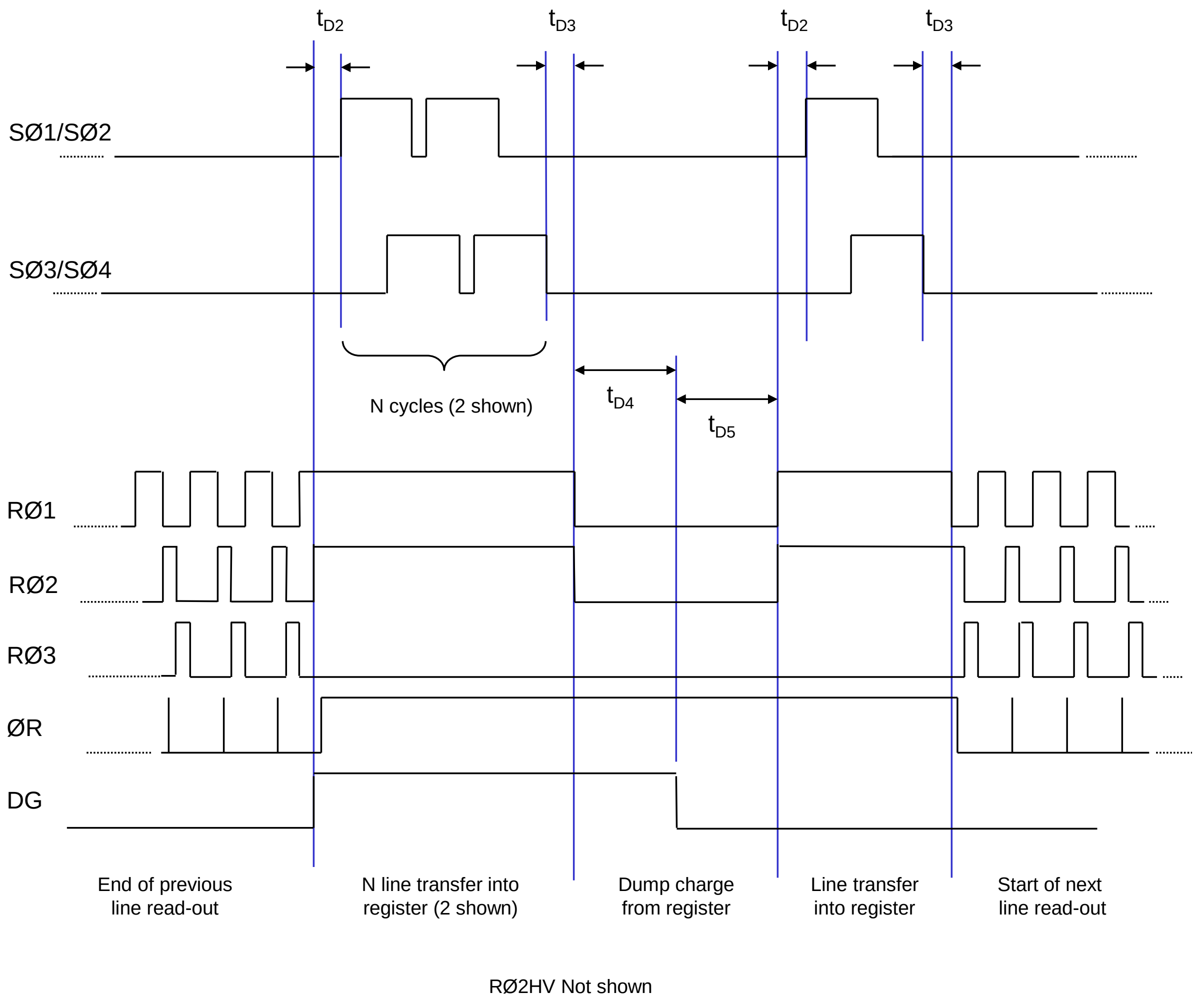
24. To operate through the OSH output amplifier, the R∅1 and R∅2 waveforms should be interchanged.

Trapezoidal Clocking Scheme

See note 23, not used for factory testing

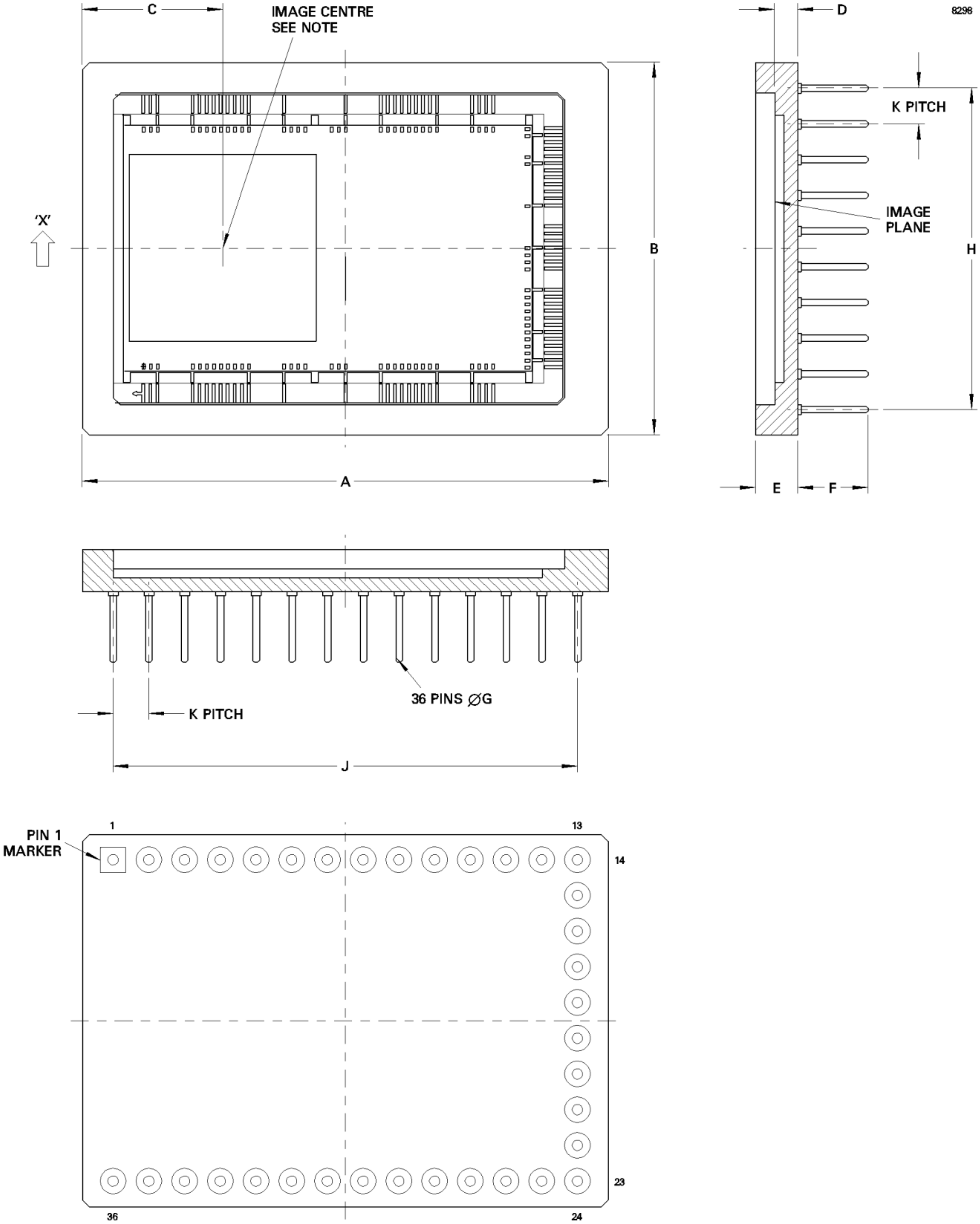


LINE DUMPING – IF REQUIRED



OUTLINE DRAWINGS

PACKAGE OUTLINE (Tolerances are by design and not verified on each part)



The image center is aligned centrally in the package in direction ‘X’, to within a tolerance of ±0.20mm.

HEALTH AND SAFETY HAZARDS

Teledyne e2v devices are safe to handle and operate, provided that the relevant precautions stated herein are observed. Teledyne e2v does not accept responsibility for damage or injury resulting from the use of devices it produces. Equipment manufacturers and users must ensure that adequate precautions are taken. Appropriate warning labels and notices must be provided on equipment incorporating Teledyne e2v devices and in operating manuals.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap.
- All receiving socket pins to be positively grounded.
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to an ionising radiation. Users planning to use CCDs in a high radiation environment are advised to contact Teledyne e2v.

TEMPERATURE LIMITS

	Min	**Typical**	**Max**
Storage...........................	-200°C	-	+100°C
Operating	-120°C	-	+75°C

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage. Full performance is only guaranteed at the nominal operating temperature of 18°C.

Maximum device heating/cooling	5	K/min

PART REFERENCES

Variant	Operating Mode	Illumination	Enhanced BSI Process	Silicon	AR Coating	Fringe Suppression	Notes
CCD201-20-G-122	L3 2-phase	BSI	No	Standard	Midband	No	
CCD201-20-G-139	L3 2-phase	BSI	No	Standard	Midband	No	25
CCD201-20-G-168	L3 2-phase	BSI	No	Standard	Broadband	No	
CCD201-20-G-171	L3 2-phase	BSI	No	Standard	Midband	Yes	
CCD201-20-G-178	L3 2-phase	BSI	No	Standard	Multi-2	No	
CCD201-20-G-179	L3 2-phase	BSI	No	Standard	Multi-2	Yes	
CCD201-20-G-185	L3 2-phase	BSI	No	Standard	UV	No	
CCD201-20-G-S29	L3 2-phase	BSI	No	Standard	Midband	No	26
CCD201-20-G-S75	L3 2-phase	BSI	Yes	Standard	Multi-19	No	

Grade Definitions

Grade 0	Super Grade	Meets all performance parameters and Grade 0 cosmetic parameters
Grade 1	Science Grade	Meets all performance parameters and Grade 1 cosmetic parameters
Grade 5	Engineering Grade	Electrically functional with no performance or cosmetic parameter guarantees
Grade 6	Mechanical Grade	Non-functional. Mechanically representative only.

NOTES

25. Lumogen coated device.
26. OSH output capability not included
27. G = Grade (e.g. 1)
28. Additional variants may be available to custom order. Consult Teledyne e2v for more information.