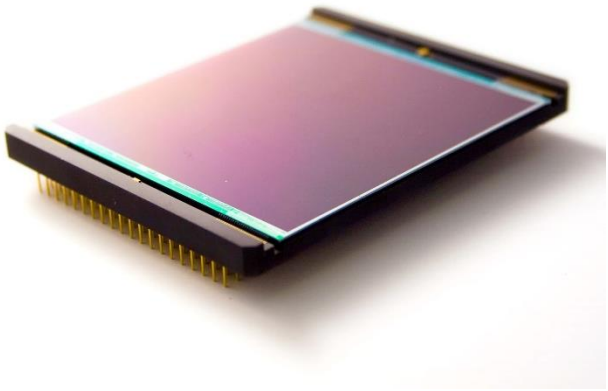
CCD230-84

16MP BSI CCD Sensor



KEY FEATURES

- 4096 x 4112 active pixels
- 15µm square pixels
- Back Illuminated
- Full-frame or frame transfer
- Advanced inverted mode operation
- Tight flatness tolerance
- Uncoated option for soft X-Ray

TYPICAL APPLICATIONS

- X-Ray Imaging
- Astronomy
- Scientific Imaging

PART REFERENCES

Please see last page for full list of available parts.

A similar version (CCD231-84) is also available with lower readout noise and buttable package options but requires additional cooling to achieve low dark signal.

GENERAL DATA

Format	
Image Area	61.4 × 61.4 mm
Active Pixels	4096(H) x 4112(V)
Pixel Size	15 × 15 µm
Number of output amplifiers	4
Package	
Package size	63.80 x 79.60 mm
Package format	Aluminium Oxide PGA
Connectors	80-pin PGA
Focal plane height, above base	3.6 mm
Performance	
Output amplifier sensitivity	2.5 µV/e^-
Typical readout noise	8 e^- at 750 kHz
Max output data rate	5 MHz
Typical pixel charge capacity	150 ke^-/pixel
Typical dark signal (-25°C)	0.2 e^-/pixel/second
Typical flatness (peak to valley)	20 µm

OVERVIEW

The CCD230-84 is a large area CCD designed for high speed and low dark current. The Teledyne e2v back-thinning process ensures high quantum efficiency over a wide range of wavelengths.

The image area has four separately connected sections to allow full-frame, frame transfer, split full-frame or split frame transfer read-out modes. Depending on the mode, the read-out can be through 1, 2 or 4 of the output circuits. A gate-controlled drain is provided to allow fast dumping of unwanted data.

The output amplifier is a two-stage type designed to give minimum noise at pixel rates as high as 5 MHz.

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Template: 1B300000-DFP Ver 1
CM5005133

Approved for public release: Teledyne e2v APPROVED (5005133)

PERFORMANCE

		Min	Typical	Max	Units	Note
Peak charge storage (image)		120,000	150,000	-	e^-/pixel	3(a)
Peak charge storage (register/SW)		-	850,000	-	e^-/pixel	2, 3(b)
Output node capacity	OG low (mode 1)	-	450,000	-	e^-	2, 3(c)
	OG high (mode 2)	-	900,000	-	e^-	
Output amplifier responsivity	mode 1	1.7	2.5	-	$\mu V/e^-$	4
	mode 2	-	0.8	-	$\mu V/e^-$	2
Readout noise	750 kHz	-	8	14	e^- rms	5
Readout frequency		-	1	5	MHz	6
Dark signal	248 K (measured)	-	0.2	2.0	e^-/pixel/s	7
Charge transfer efficiency	Parallel	99.9990	99.9995	-	%	8
	Serial	99.9990	99.9995	-	%	

NOTES

1. Device performance will be within the limits specified by “max” and “min” when operated at the recommended voltages supplied with the test data and when measured at a register clock frequency of approximately 0.5 – 1.0 MHz. Most test are performed at a nominal 500 kHz. The noise as specified is separately measured in accordance with note 5.
2. Not measured as production test.
3. (a) Signal level at which resolution begins to degrade.

   (b) The summing well capacity limits the charge in the register.

   (c) The signal handled by the output node (for linear operation) varies with mode as shown. Values are inferred by design and not factory tested.
4. Under normal operation (mode 1), SW is operated as a summing well or clocked as RØ3. OG is biased at typically 2 V. Alternatively, SW may be operated as a second output gate (and not therefore available for summing), biased at typically 2 V with OG raised to a high voltage (mode 2) to give more charge handling capacity (e.g. for higher level pixel binning). With OG high, the output noise will also increase by a factor of two.
5. Measured with correlated double sampling at 750 kHz pixel rate.
6. Depending on the external load capacitance to be driven. The register will transfer charge at higher frequencies, but performance cannot be guaranteed.
7. Dark signal is typically measured at a device temperature of 173 K. It is a strong function of temperature and the typical average (background) dark signal at any temperature T (Kelvin) between 150 K and 300 K is given by:

   $Q_d/Q_{do} = 1.14 \times 10^6 T^3 e^{-9080/T}$

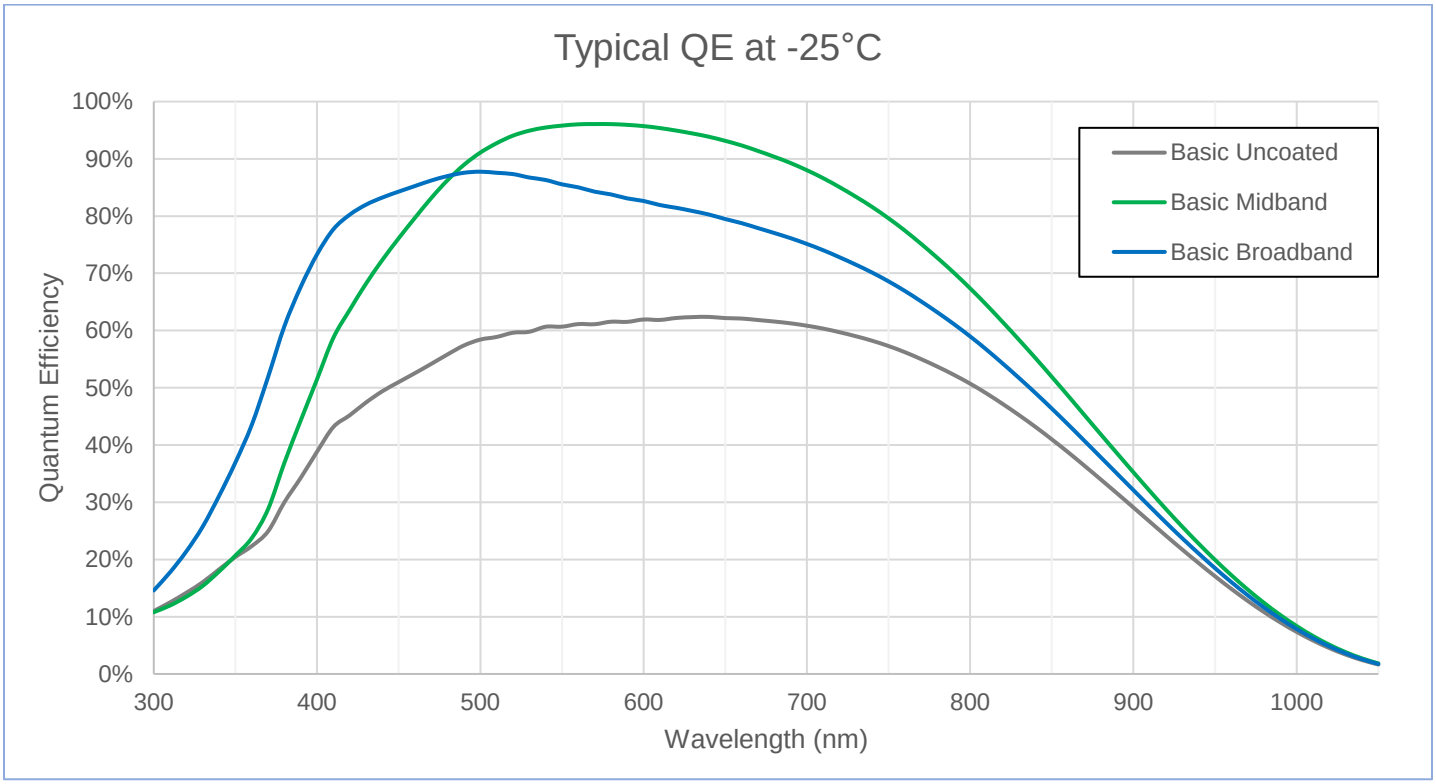
   where Q_{do} is the dark current at 293 K.

   Transfer through the image sections can give rise to an additional temperature-independent component of “clock-induced charge” with of a magnitude in the region of 10^{-4} electrons per pixel transfer.
8. Measured with a ^{55}Fe X-ray source. The CTE value is quoted for the complete clock cycle (i.e. not per phase).

SPECTRAL RESPONSE

The table below gives guaranteed minimum values of the spectral response at -25°C.

Wavelength (nm)	Minimum Response (QE)			Max PRNU (1 σ)	
	Broadband Coated	Midband Coated	Uncoated		
350	25	15	10	5	**%**
400	55	40	25	3	**%**
500	75	85	50	3	**%**
650	75	85	55	3	**%**
900	25	25	25	5	**%**



v

NOTES

9. Devices with alternative or custom spectral response may be available by special request. Consult Teledyne e2v.

COSMETIC SPECIFICATIONS

Maximum allowed defect levels are indicated below.

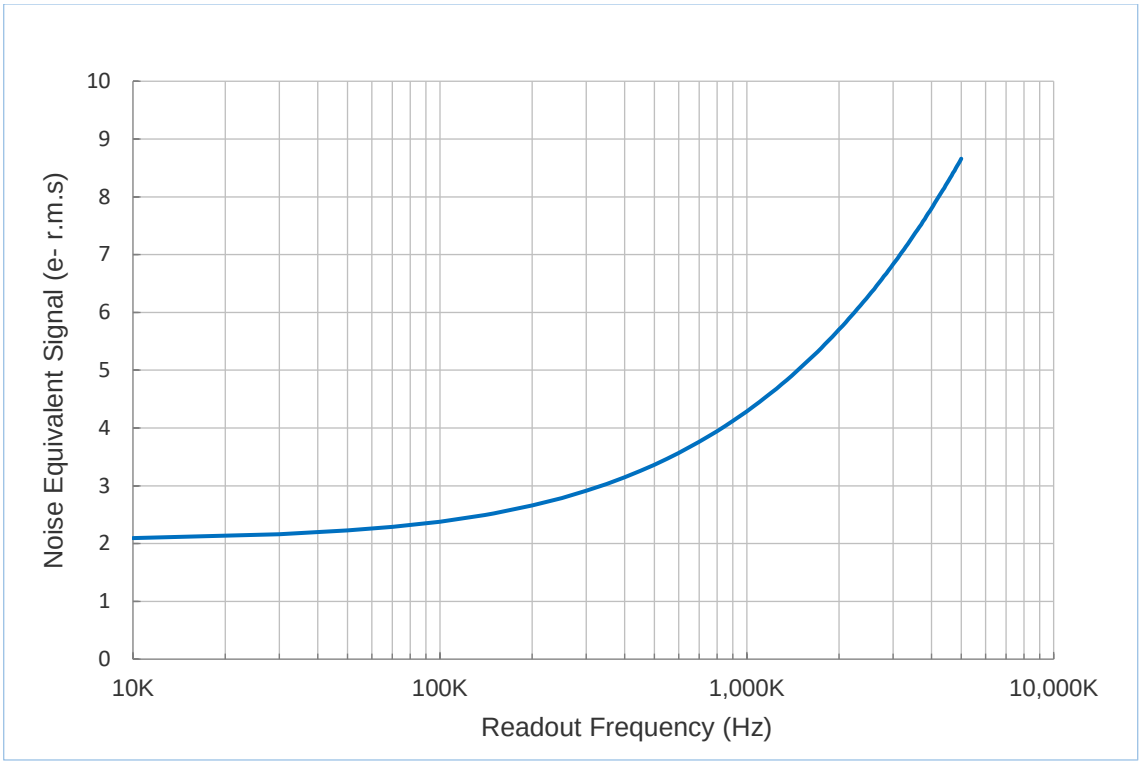
Grade		0	1	2
Column defects	Black or White	5	10	20
	Adjacent	0	2	4
White spots		400	800	1200
Total (black & white) spots		800	1500	2000
Traps > 200e-		10	20	30

Cosmetic definitions

White spots	A defect is counted as a white spot if the dark generation rate is ≥ 500 e-/pixel/s at 248 K. The temperature dependence is the same as for the mean dark signal; see note 7 above.
Black spots	A black spot defect is a pixel with a photo-response less than 80% of the local mean.
Column defects	A column is counted as a defect if it contains at least 50 white or dark single pixel defects.
Traps	A trap causes charge to be temporarily held in a pixel and these are counted as defects if the quantity of trapped charge is greater than 200 e-.
Defect exclusion zone	Defect measurements are excluded from the outer two rows and columns of the sensor.

AMPLIFIER READ NOISE

The theoretical variation of read noise with operating frequency is shown below. (If measured using correlated double sampling with a pre-sampling bandwidth equal to twice the pixel rate in mode 1 at approximately 248 K).



DEFINITIONS

Back-thinning

A back-thinned CCD is fabricated on the front surface of the silicon and is subsequently processed for illumination from the reverse side. This avoids loss of transmission in the electrode layer (particularly significant at shorter wavelengths or with low energy X-rays). This process requires the silicon to be reduced to a thin layer by a combination of chemical and mechanical means. The surface is “passivated” and an anti-reflection coating may be added.

AR Coating

Anti-reflection coatings are normally applied to the back illuminated CCD to further improve the quantum efficiency. Standard coatings optimise the response in the visible, ultra-violet or infrared regions. For X-ray detection an uncoated device may be preferable.

Inverted Mode

An inverted mode CCD has an additional implant that allows charge integration to be carried out with all clock phases low. With a high voltage applied to the substrate (typically +9 V) this causes the whole of the device to be flooded with holes (inverted or pinned), which suppresses the surface component of dark signal. This leaves only the much lower bulk component, reducing the overall dark signal by a factor of approximately 100.

Inverted mode operation is also referred to as multi-phase pinning (MPP).

Readout Noise

Readout noise is the random noise from the CCD output stage in the absence of signal. This noise introduces a random fluctuation in the output voltage that is superimposed on the detected signal.

The method of measurement involves reverse-clocking the register and determining the standard deviation of the output fluctuations, and then converting the result to an equivalent number of electrons using the known amplifier responsivity.

Dummy Output

Each output has an associated “dummy” circuit on-chip, which is of identical design to the “real” circuit but receives no signal charge. The dummy output should have the same levels of clock feed-through and can thus be used to suppress the similar component in the “real” signal output by means of a differential pre-amplifier. The penalty is that the noise is increased by a factor of $\sqrt{2}$. If not required, the dummy outputs may be powered down.

Dark Signal

This is the output signal of the device with zero illumination. This typically consists of thermally generated electrons within the semiconductor material, which are accumulated during signal integration. Dark signal is a strong function of temperature as described in note 7.

Correlated Double Sampling

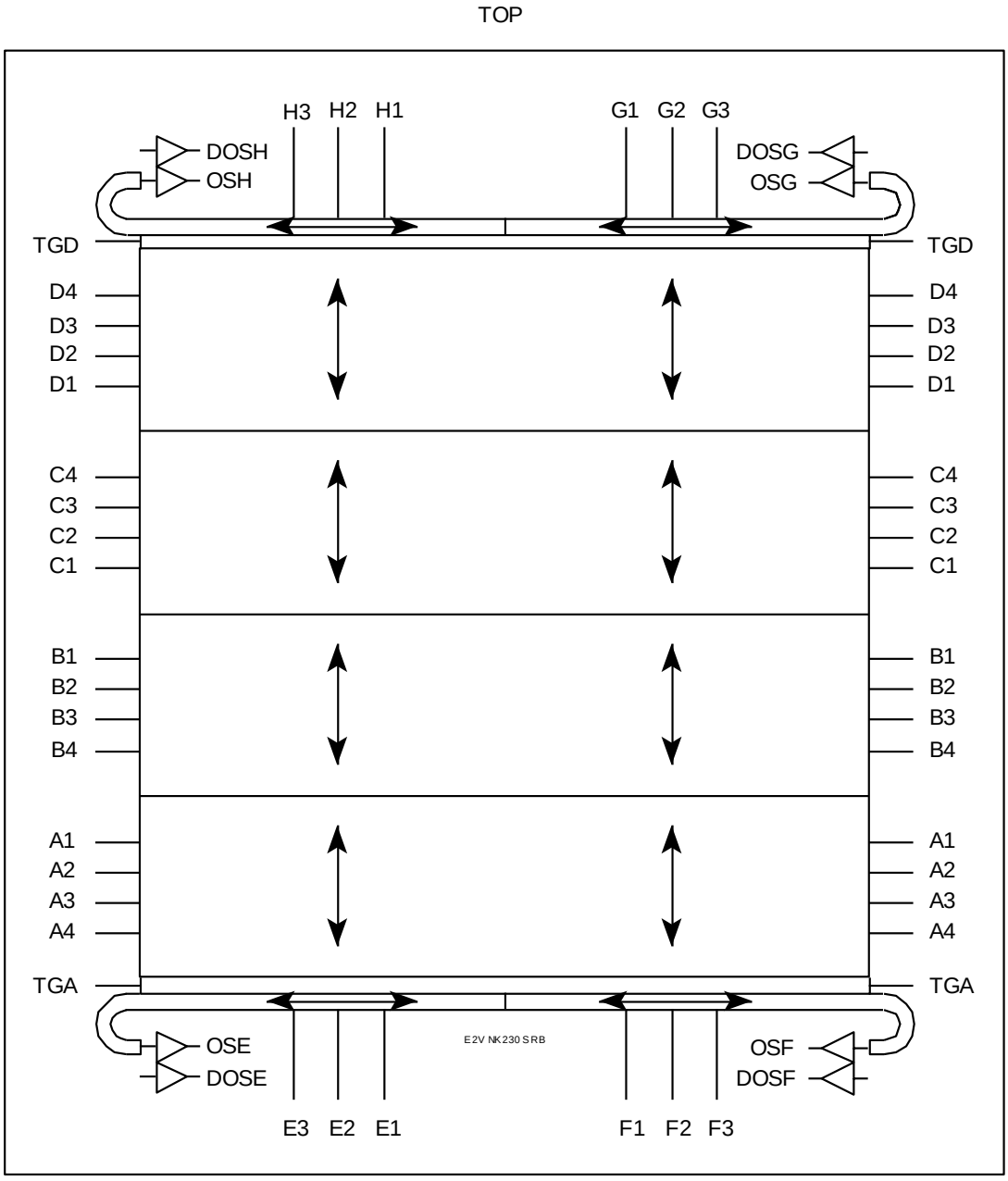
A technique for reducing the noise associated with the charge detection process by subtracting a first output sample taken just after reset from a second sample taken with charge present.

Charge Transfer Efficiency

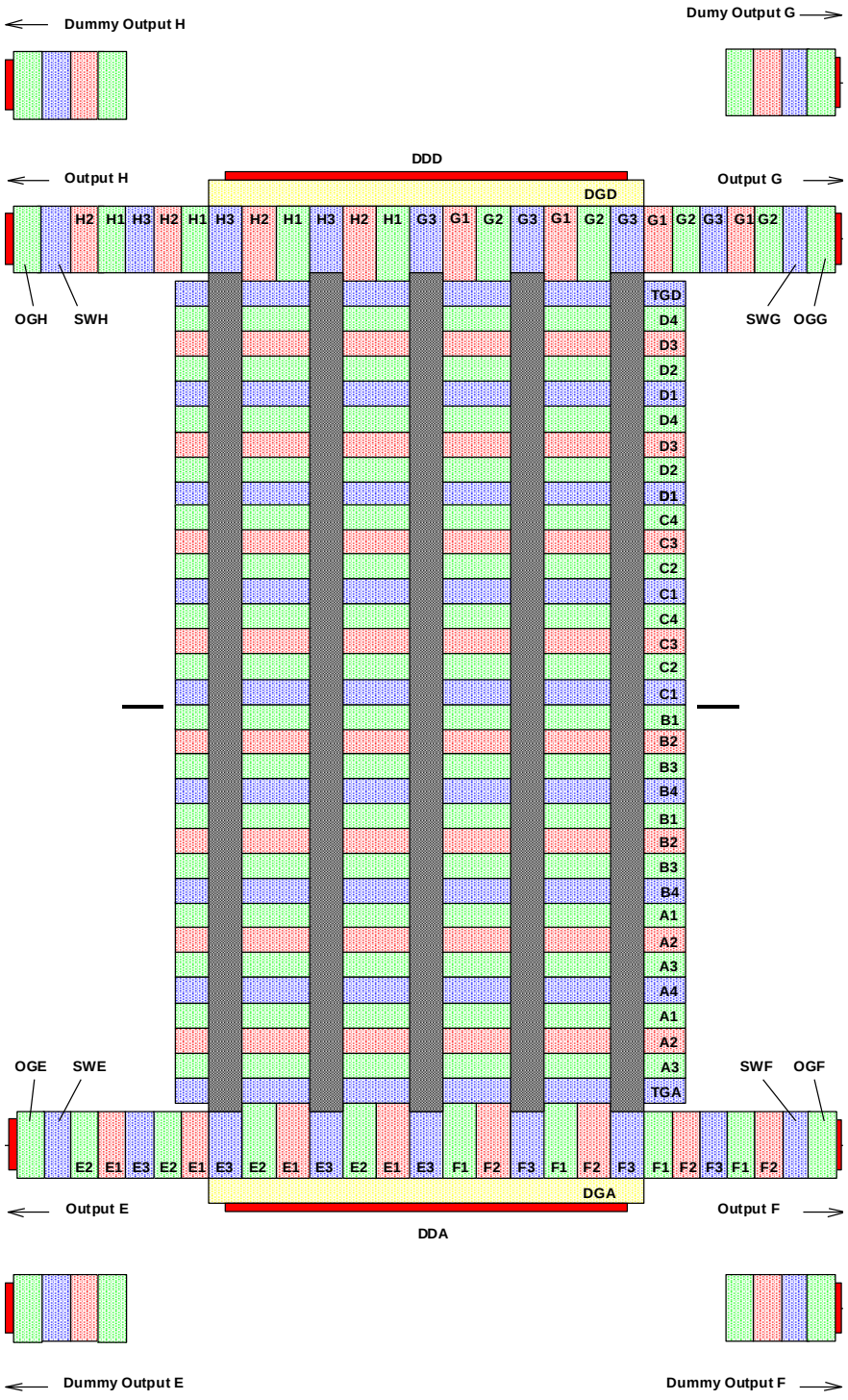
The fraction of charge stored in a CCD element that is transferred to the adjacent element by a single clock cycle. The charge not transferred remains in the original element, possibly in trapping states and may possibly be released into later elements. The value of CTE is not constant but varies with signal size, temperature, and clock frequency.

ARCHITECTURE

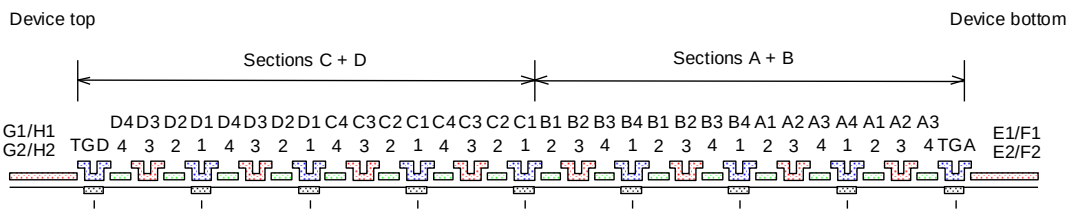
Chip Schematic



ARRANGEMENT OF ELECTRODES

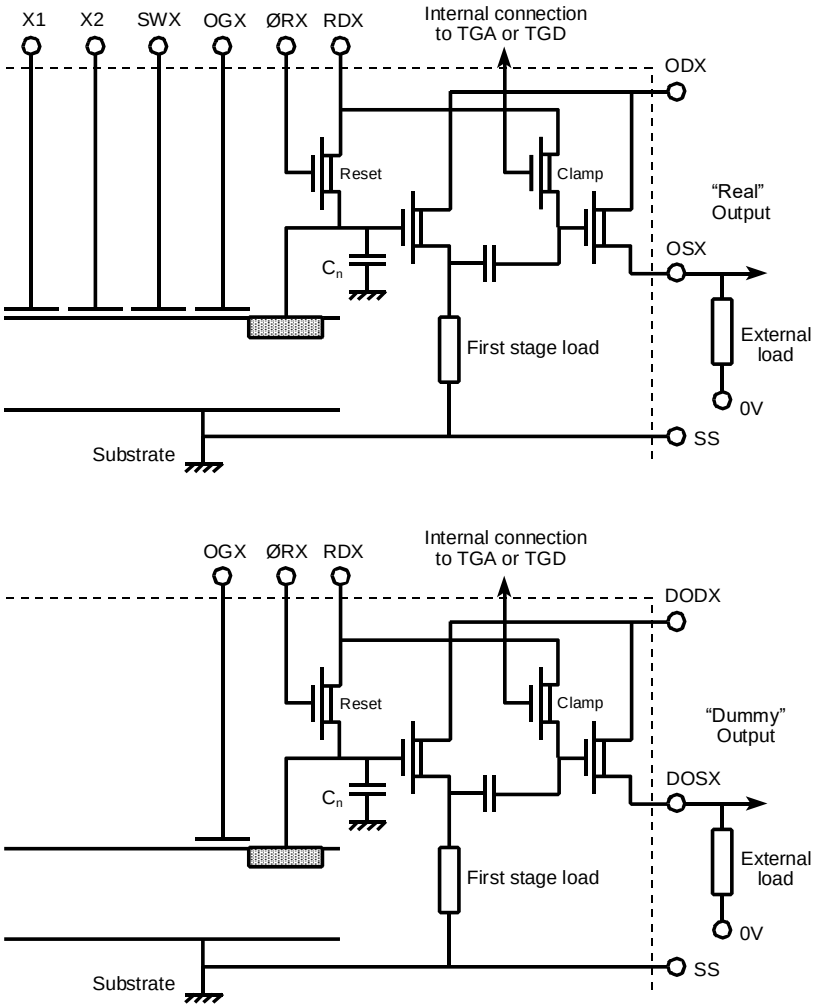


The IMO implant is under image phases A4, B4, C1, D1 and the transfer gates as shown below.



OUTPUT CIRCUIT

X designates a specific output, namely E, F, G or H.



The first stage load of each output (real or dummy) draws a quiescent current of approximately 0.3 mA.

The output circuit consists of two capacitor-coupled source-follower stages. This particular design has a reduced responsivity to allow binning of large charge packets. The load for the first stage is on-chip and that for the second stage is external, as next described. The DC restoration circuitry requires a pulse at the start of line readout, and this is automatically obtained by an internal connection to the adjacent transfer gate, TG. Transferring a line of charges to the register thus automatically activates the circuitry. N.B. TG pulses still need to be applied at similar intervals if only the register and/or output circuit are being operated, e.g. for test or characterisation purposes.

If an output is to be powered down, it is recommended that either OD or DOD be set to SS voltage, taking care that the maximum ratings are never exceeded or that OD and DOD be disconnected. If external loads return to a voltage below SS they should also be disconnected.

ELECTRICAL INTERFACE

CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

Note that the hyphenated suffix symbols (e.g. ∅R-H) indicate to which output any register or amplifier pin relates.

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 12)			MAX RATINGS with respect to V_{SS} (V)
			Min	Typical	Max	
1	DOS-E	Dummy Output Source (E)		(see note 10)		-0.3 to +25
2	DOD-E	Dummy Output Drain (E)	27	30	31	29
3	OS-E	Output Source (E)		(see note 10)		-0.3 to +25
4	OD-E	Output Drain (E)	27	30	31	-0.3 to +35
5	RD-E	Reset Drain (E)	16	18	19	-0.3 to +25
6	SS	Substrate	8	9	10.5	N/A
7	OG-E	Output Gate (E) (see note 11)	1	4	5	±20
8	SW∅-E	Summing Well (E) (see note 11)	9	11	12	±20
9	E3	Register Clock Phase 3 (E)	9	11	12	±20
10	∅R-E	Reset Gate (E)	9	11	12	±20
11	E2	Register Clock Phase 2 (E)	9	11	12	±20
12	E1	Register Clock Phase 1 (E)	9	11	12	±20
13	A1	Image Area Clock Phase 1 (A)	9	11	12	±20
14	SS	Substrate	8	9	10.5	N/A
15	A2	Image Area Clock Phase 2 (A)	9	11	12	±20
16	A3	Image Area Clock Phase 3 (A)	9	11	12	±20
17	SS	Substrate	8	9	10.5	N/A
18	A4	Image Area Clock Phase 4 (A)	9	11	12	±20
19	TS-1	Temperature Sensor 1 – Pin 1		(see note 14)		N/A
20	DG-A	Dump Gate (A) (see note 13)	-2	0	0.5	±20
21	TS-2	Temperature Sensor 1 – Pin 2		(see note 14)		N/A
22	DD-A	Dump Drain (A)	27	30	31	-0.3 to +35
23	TG-A	Transfer Gate (A)	9	11	12	±20
24	B4	Image Area Clock Phase 4 (B)	9	11	12	±20
25	B2	Image Area Clock Phase 2 (B)	9	11	12	±20
26	B3	Image Area Clock Phase 3 (B)	9	11	12	±20
27	B1	Image Area Clock Phase 1 (B)	9	11	12	±20
28	SS	Substrate	8	9	10.5	N/A
29	F1	Register Clock Phase 1 (F)	9	11	12	±20
30	F2	Register Clock Phase 2 (F)	9	11	12	±20
31	F3	Register Clock Phase 3 (F)	9	11	12	±20
32	∅R-F	Reset Gate (F)	9	11	12	±20
33	OG-F	Output Gate (F) (see note 11)	1	4	5	±20
34	SW∅-F	Summing Well (F) (see note 11)	9	11	12	±20
35	RD-F	Reset Drain (F)	16	18	19	-0.3 to +25
36	SS	Substrate	8	9	10.5	N/A
37	OS-F	Output Source (F)		(see note 10)		-0.3 to +25
38	OD-F	Output Drain (F)	27	30	31	-0.3 to +35
39	DOS-F	Dummy Output Source (F)		(see note 10)		-0.3 to +25
40	DOD-F	Dummy Output Drain (F)	27	30	31	-0.3 to +35

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 17)			MAX RATINGS with respect to V_{SS} (V)
			Min	Typical	Max	
41	DOS-G	Dummy Output Source (G)		(see note 10)		-0.3 to +25
42	DOD-G	Dummy Output Drain (G)	27	30	31	29
43	OS-G	Output Source (G)		(see note 10)		-0.3 to +25
44	OD-G	Output Drain (G)	27	30	31	-0.3 to +35
45	RD-G	Reset Drain (G)	16	18	19	-0.3 to +25
46	SS	Substrate	8	9	10.5	N/A
47	OG-G	Output Gate (G) (see note 11)	1	4	5	±20
48	SW∅-G	Summing Well (G) (see note 11)	9	11	12	±20
49	G3	Register Clock Phase 3 (G)	9	11	12	±20
50	∅R-G	Reset Gate (G)	9	11	12	±20
51	G2	Register Clock Phase 2 (G)	9	11	12	±20
52	G1	Register Clock Phase 1 (G)	9	11	12	±20
53	D4	Image Area Clock Phase 4 (D)	9	11	12	±20
54	SS	Substrate	8	9	10.5	N/A
55	D3	Image Area Clock Phase 3 (D)	9	11	12	±20
56	D2	Image Area Clock Phase 2 (D)	9	11	12	±20
57	SS	Substrate	8	9	10.5	N/A
58	D1	Image Area Clock Phase 1 (D)	9	11	12	±20
59	TS-3	Temperature Sensor 2 – Pin 1		(see note 14)		N/A
60	DG-D	Dump Gate (D) (see note 13)	-2	0	0.5	±20
61	TS-4	Temperature Sensor 2 – Pin 2		(see note 14)		N/A
62	DD-D	Dump Drain (D)	27	30	31	-0.3 to +35
63	TG-D	Transfer Gate (D)	9	11	12	±20
64	C1	Image Area Clock Phase 1 (C)	9	11	12	±20
65	C3	Image Area Clock Phase 3 (C)	9	11	12	±20
66	C2	Image Area Clock Phase 2 (C)	9	11	12	±20
67	C4	Image Area Clock Phase 4 (C)	9	11	12	±20
68	SS	Substrate	8	9	10.5	N/A
69	H1	Register Clock Phase 1 (H)	9	11	12	±20
70	H2	Register Clock Phase 2 (H)	9	11	12	±20
71	H3	Register Clock Phase 3 (H)	9	11	12	±20
72	∅R-H	Reset Gate (H)	9	11	12	±20
73	OGH	Output Gate (H) (see note 11)	1	4	5	±20
74	SW∅-H	Summing Well (H) (see note 11)	9	11	12	±20
75	RD-H	Reset Drain (H)	16	18	19	-0.3 to +25
76	SS	Substrate	8	9	10.5	N/A
77	OS-H	Output Source (H)		(see note 10)		-0.3 to +25
78	OD-H	Output Drain (H)	27	30	31	-0.3 to +35
79	DOS-H	Dummy Output Source (H)		(see note 10)		-0.3 to +25
80	DOD-H	Dummy Output Drain (H)	27	30	31	-0.3 to +35

NOTES

10. Do not connect to voltage supply but use a ~5 mA current source or a ~5 kΩ external load. The quiescent voltage on OS is then about 6 - 8 V above the reset drain voltage and is typically 24 V. The current through these pins must not exceed 20 mA. Permanent damage may result if, in operation, OS or DOS experience short circuit conditions.

    For highest speed operation the output load resistor can be reduced from 5 kΩ to approximately 2.2 kΩ, but note that this will increase power consumption. If the device is to be operated with a register clock period of below about 1 MHz then the load may be increased to 10 kΩ to reduce power consumption.

    In order to ensure that the amplifier is well settled the output load capacitance should be minimised (typically <20 pF) for the highest readout rate.

11. Default operation (mode 1) shown with OG at +2 V typical. In this mode SW may be clocked as R∅3 if a summing well function is not required.

    For alternative operation in a low responsivity mode with increased charge handling, OG should be set to +20 V and SW should be operated as OG. Charge is now read out as R∅2 goes low.

12. To ensure that any device can be operated the camera should be designed so that any value in the range “min” to “max” can be provided. All operating voltages are with respect to image clock low (nominally 0 V).

    The clock pulse low levels should be in the range 0 ± 0.5 V for image, register, SW and DG clocks.

13. Non-charge dumping level shown. For charge dumping, DG should be pulsed to 12 ± 2 V (this may be provided from a common rail to the register clocks).

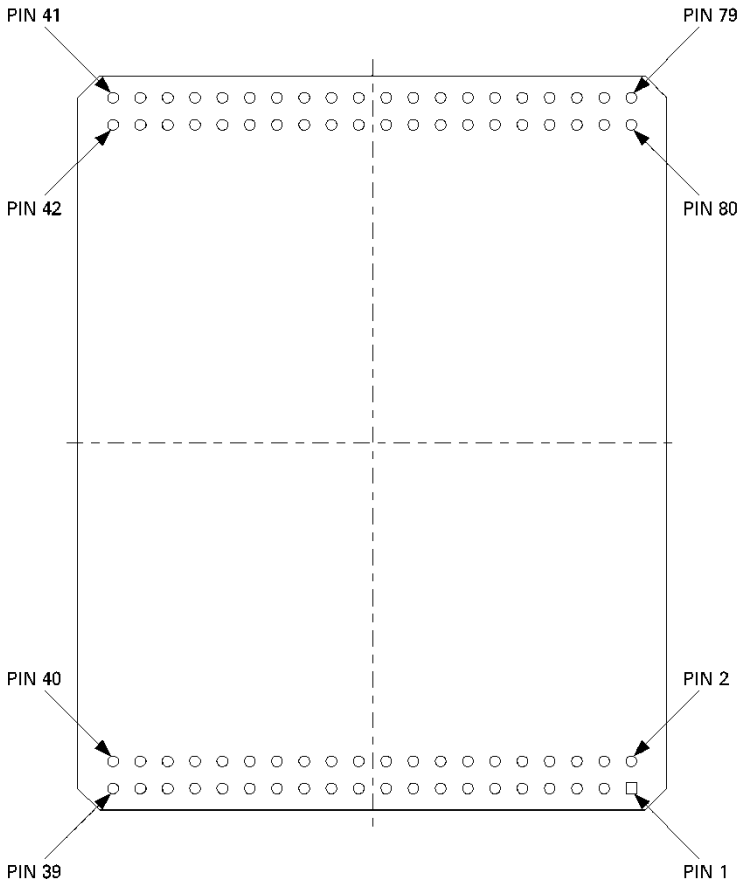
14. Two Fenwal NTC 196-LAD302-002 negative temperature coefficient thermistors are provided in the package for thermal control purposes.

15. This data sheet assumes that all signals are relative to the clock low level of 0V. The absolute level for all biases and clock rails may be changed to suit the needs of the designer provided the relative levels are maintained. For example, it is acceptable to set Vss to 0 V so long as the specified difference between Vss and all other bias and clock voltages is maintained and the current load on all output sources is as recommended in note 10.

16. DD and OD may be provided from a common rail provided that they are separately filtered sufficiently to ensure that there is no clock pick-up on OD.

17. Image and register clock high voltages may be provided from common rails.

PIN CONNECTIONS (View facing pins of connector)



ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (defined at mid-clock level)

	Typical	Units
I∅/I∅ inter-phase [A, B, C and D]	10	nF
I∅/SS [A1, A2, A3, B1, B2, B3, C2, C3, C4, D2, D3, D4)	20	nF
I∅/SS [4-A, 4-B, 1-C, 1-D]	50	nF
Transfer gates [TGA, TGD]	130	pF
R∅/(SS + DG + DD) [E1, F1, G1, H1]	190	pF
R∅/(SS + DG + DD) [E2, F2, G2, H2]	175	pF
R∅/(SS + DG + DD) [E3, F3, G3, H3]	155	pF

The total capacitance on each phase is the sum of the inter-phase capacitance to each of the adjacent phases and the capacitance of the phase to substrate. For example, the total capacitance on phase A1 is 2 times 10 nF plus 20 nF for a total of 40 nF.

The amplifier output impedance is typically 400 Ω.

POWER UP/POWER DOWN

When powering the device up or down it is critical that any specified maximum rating is not exceeded. Specifically the voltages for the amplifier and dump drains (OD, RD, DD) must never be taken negative with respect to the substrate. Hence, if the substrate is to be operated at a positive voltage (e.g. to minimise dark current) then the drive electronics should have a switch-on sequence which powers up all the drains to their positive voltages before the substrate voltage starts to increase from zero.

It is also important to ensure that excess currents (see note 10) do not flow in the OS or DOS pins. Such currents could arise from rapid charging of a signal coupling capacitor or from an incorrectly biased DC-coupled preamplifier.

Similarly, for powering down, the substrate must be taken to zero voltage before the drains.

POWER CONSUMPTION

The power dissipated within the CCD is a combination of the static dissipation of the amplifiers and the dynamic dissipation from the parallel and serial clocking (i.e. driving the capacitive loads).

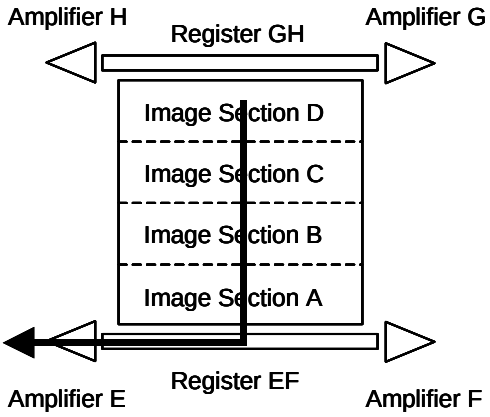
The table below gives representative values for the components of the on-chip power dissipation for the case of continuous split-frame line-by-line read-out using both registers and all the output circuits with both real and dummy amplifiers activated. The frequency is that for clocking the serial register and an appropriate value of the amplifier load is utilised in each case.

The dissipation reduces to only that of the amplifiers during the time that charge is being collected in the image sections with both the parallel and serial clocks static.

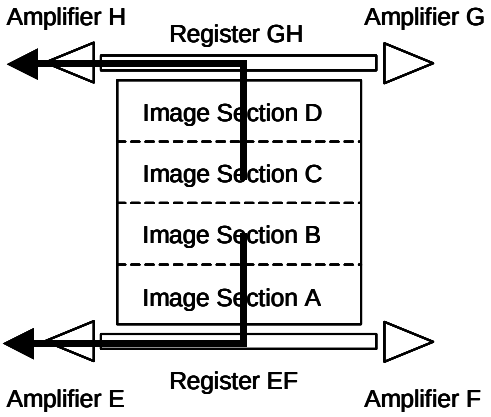
Readout frequency	Line time	Amplifier load	Power dissipation			
			Amplifiers	Serial clocks	Parallel clocks	Total
100 kHz	21 ms	10 kΩ	165 mW	17 mW	3 mW	185 mW
1 MHz	2.2 ms	5 kΩ	275 mW	170 mW	30 mW	475 mW
3 MHz	800 µs	2.2 kΩ	525 mW	510 mW	90 mW	1,125 mW

FRAME READOUT MODES

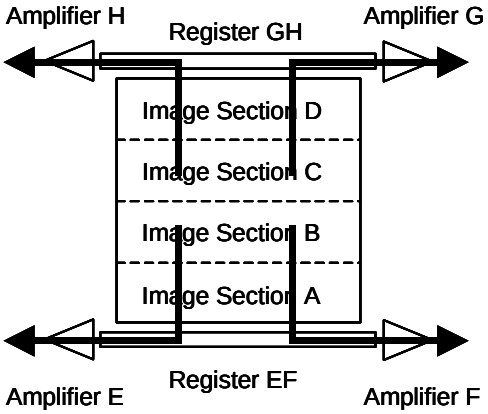
The device can be operated in a full-frame or frame transfer mode with readout from one, two or four amplifiers. These modes are determined by the clock pulse sequences applied to the image and register clocks. The diagrams below show some of the transfer options that are possible.



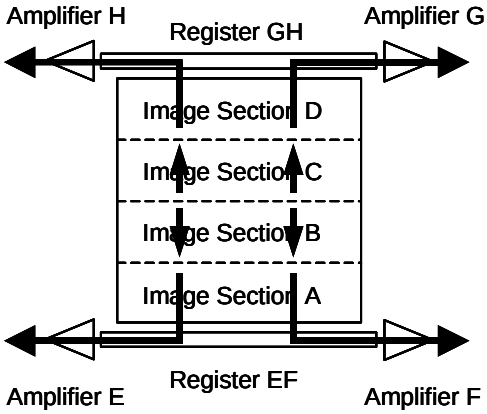
Full frame read-out through one amplifier



Split full frame read-out through two amplifiers



Split full frame read-out through four amplifiers



Split frame transfer through four amplifiers

If the applied drive pulses are designated I∅1, I∅2, I∅3 and I∅4, then connections should be made as tabulated below to affect the following directions of transfer.

	IØ1	IØ2	IØ3	IØ4	
A section transfer towards E-F register	A4	A1	A2	A3	TGA = I∅4
B section transfer towards E-F register	B4	B1	B2	B3	
C section transfer towards G-H register	C1	C2	C3	C4	
D section transfer towards G-H register	D1	D2	D3	D4	TGD = I∅1
A section transfer towards G-H register	A4	A3	A2	A1	TGA = “low”
B section transfer towards G-H register	B4	B3	B2	B1	
C section transfer towards E-F register	C1	C4	C3	C2	
D section transfer towards E-F register	D1	D4	D3	D2	TGD = “low”

The first four transfer sequences are for split frame readout. The second four are for reversing the transfer direction in either section for readout to only one of the registers.

Transfer from the image section to the register is into the phase 1 and 2 electrodes, i.e. E1, F1, G1, H1, E2, F2, G2 and H2. These electrodes must be held at clock “high” level during the process. If the register pulses are designated R∅1, R∅2 and R∅3, then connections should be made as tabulated below to affect the following directions of transfer.

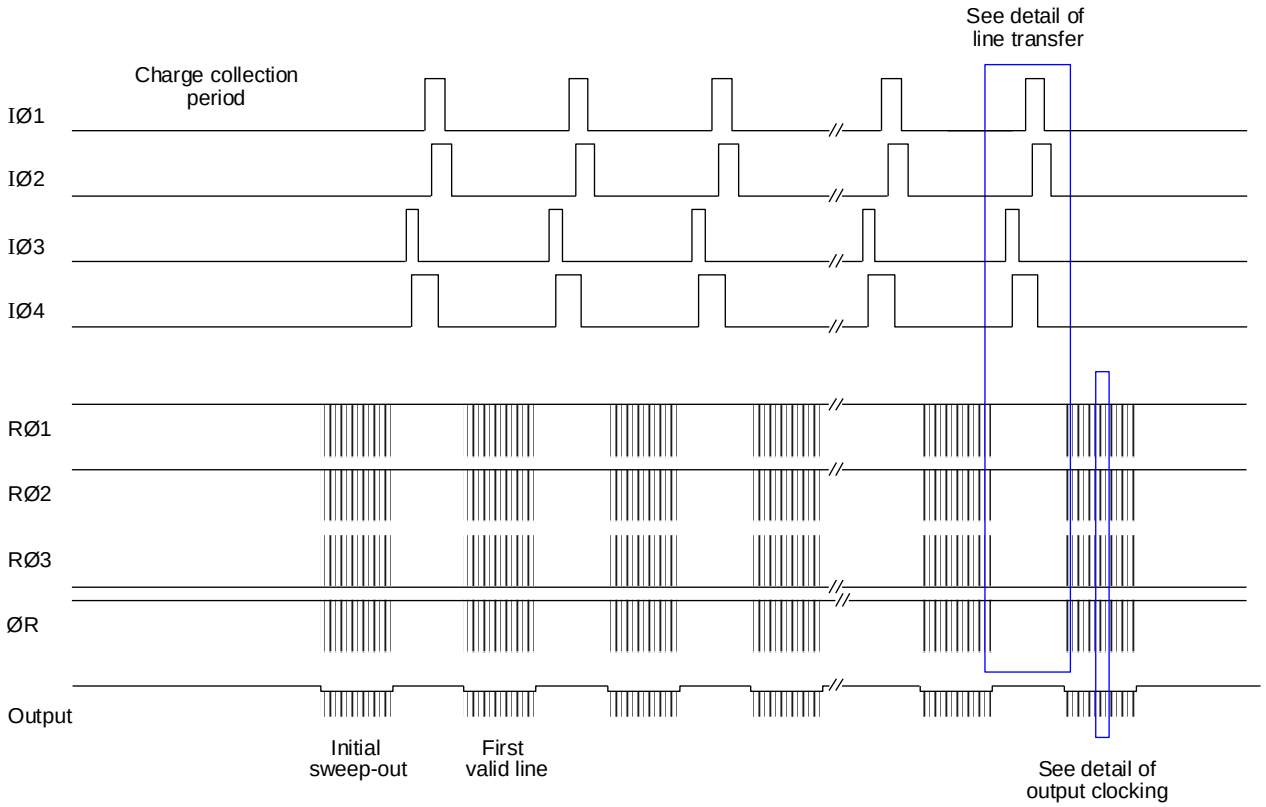
Clock Generator Drive Pulse Name	RØ1	RØ2	RØ3
E section transfer towards E output	E2	E1	E3
F section transfer towards F output	F2	F1	F3
G section transfer towards G output	G2	G1	G3
H section transfer towards H output	H2	H1	H3
E section transfer towards F output	E1	E2	E3
F section transfer towards E output	F1	F2	F3
G section transfer towards H output	G1	G2	G3
H section transfer towards G output	H1	H2	H3

The first four sequences are for split register readout to all four outputs. The second four are for the reversal of direction in any half-section.

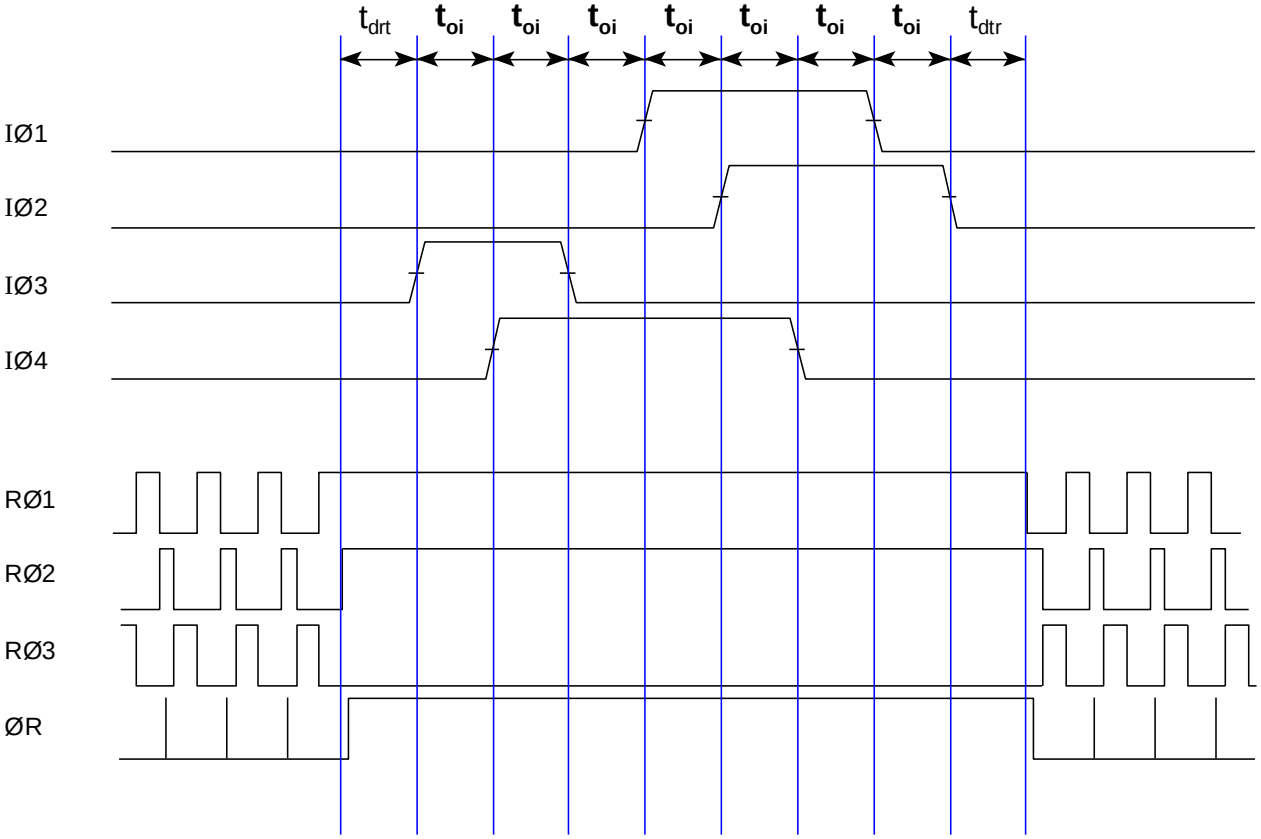
The last electrode before the output gate is separately connected to give the function of a summing well (SW). In normal readout (i.e. if not used for summing), SW is clocked as R∅3. For summing, the selected SW gate is held at clock “high” level for the required number of readout cycles, and then clocked as R∅3 to output charge.

Alternatively, SW may be operated as a second output gate to provide the option of operation in low gain/high signal mode (mode 2) with OG high. If this mode of operation is used, then the sequencing of the output clocks must be changed, as charge will be transferred into the output node as R∅2 goes low (see note 10).

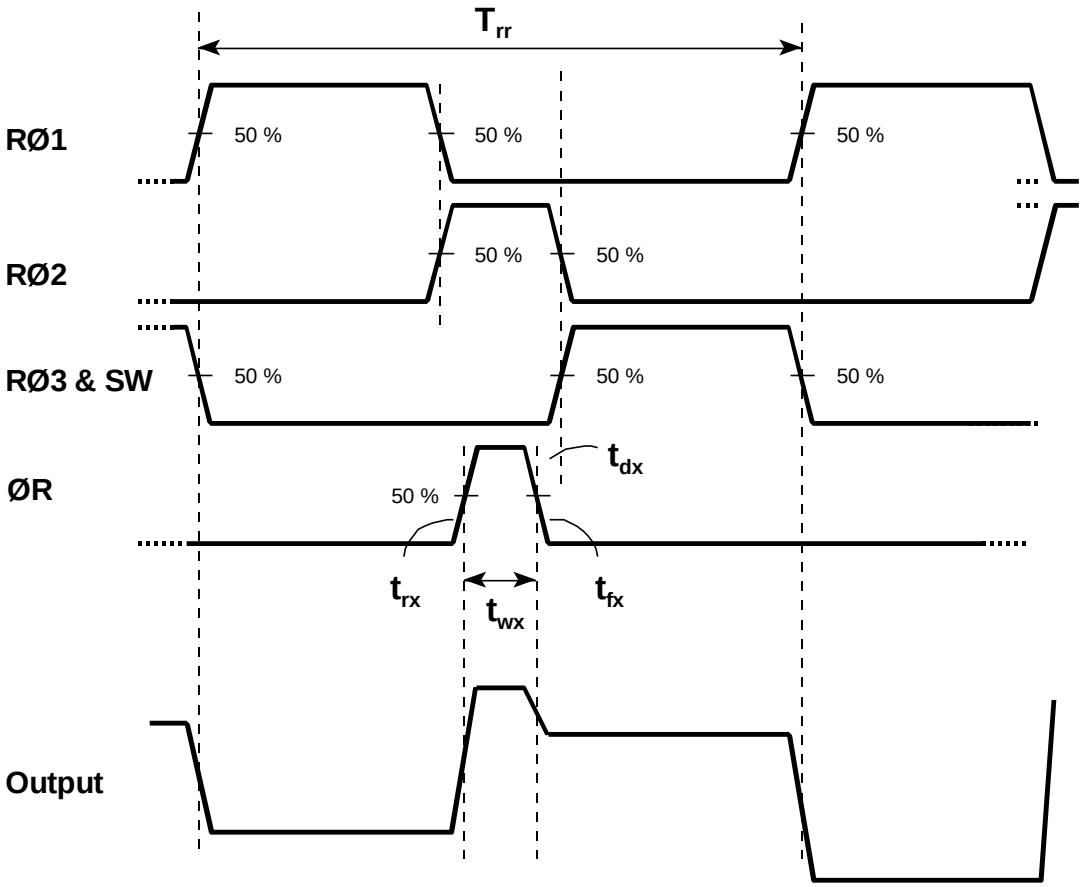
FRAME READOUT TIMING DIAGRAM

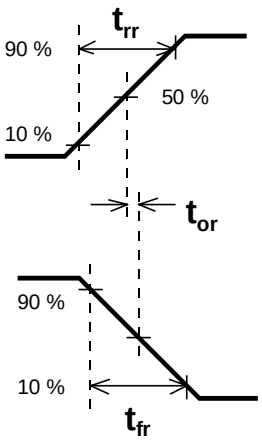


DETAIL OF LINE TRANSFER



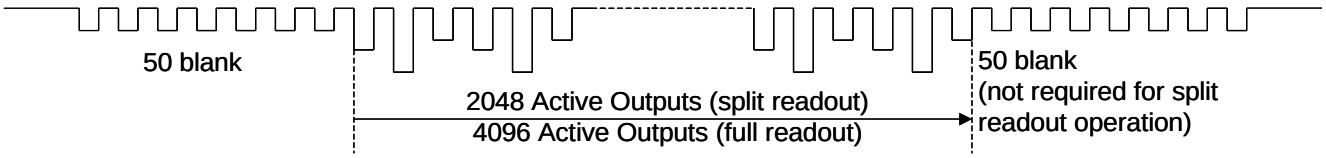
DETAIL OF OUTPUT CLOCKING (with SW clocked as RØ3)



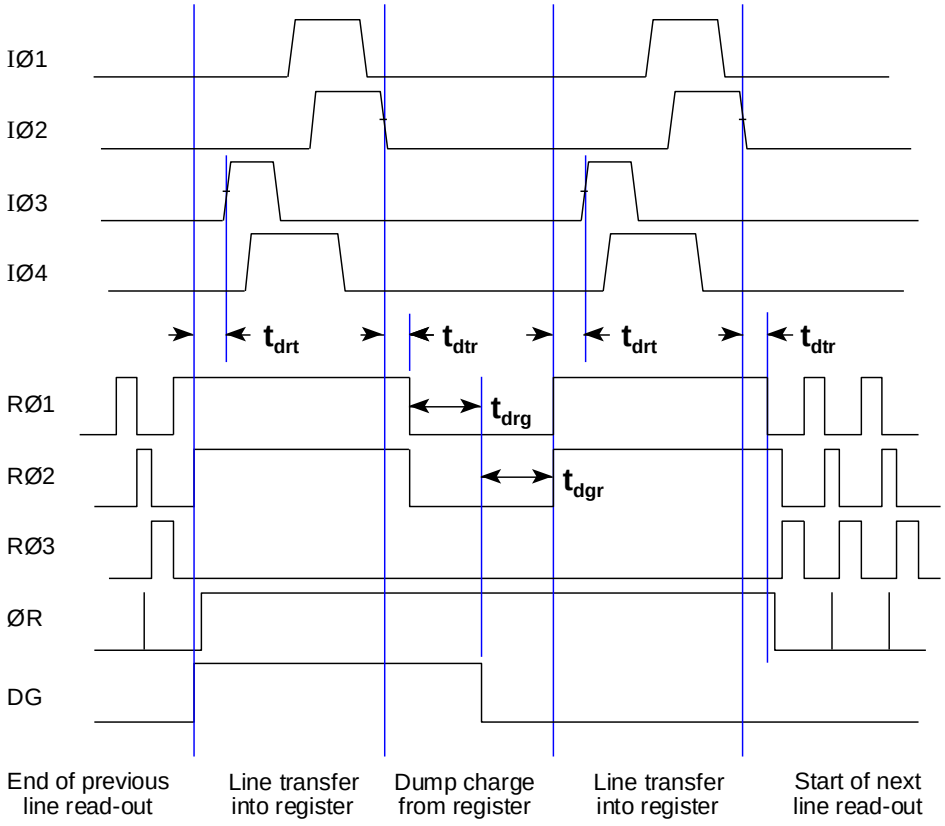


RØ Edge overlaps

LINE OUTPUT FORMAT



DETAIL OF VERTICAL LINE TRANSFER (Single line dump)



CLOCK TIMING REQUIREMENTS

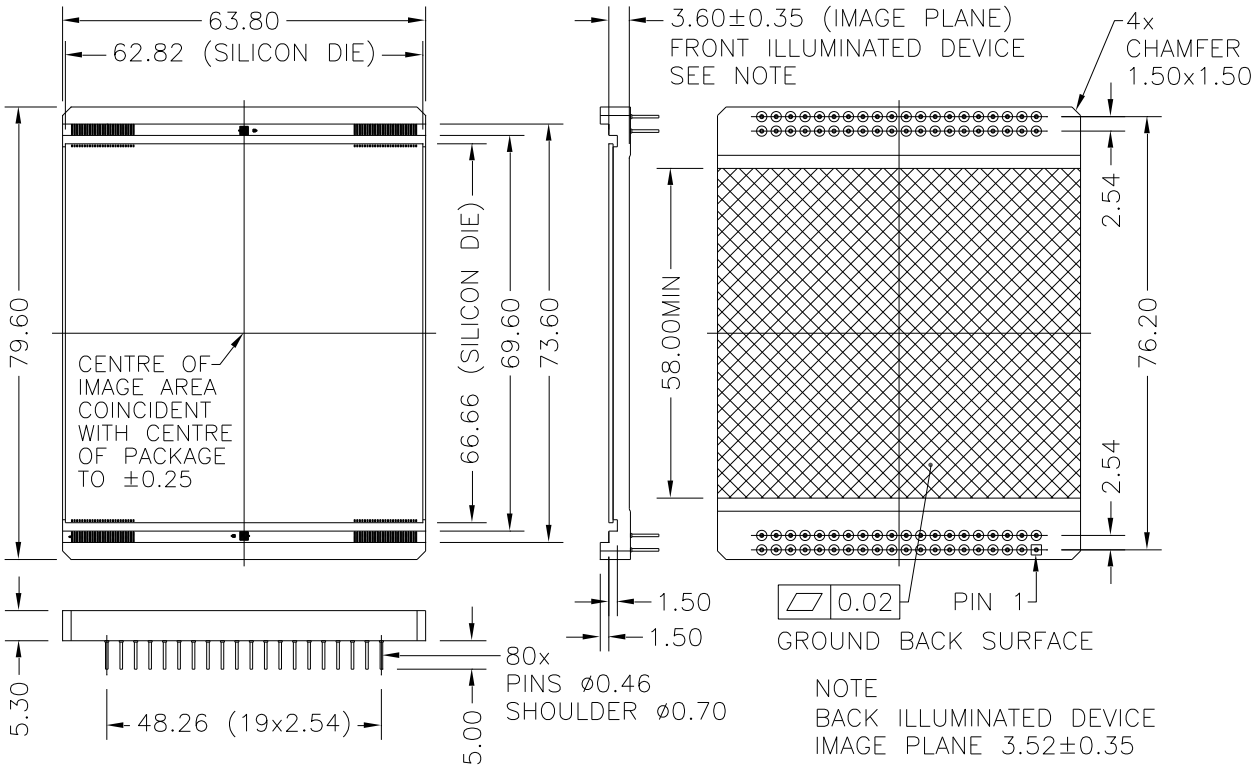
Symbol	Description	Minimum	Typical	Maximum	Units
Ti	Line transfer time (see note 18)	110	540	(see note 20)	µs
toi	Image clock pulse edge overlap	12	60	(see note 20)	µs
tri	Image clock and transfer gate pulse rise time	1	2	0.3 toi	µs
tfi	Image clock pulse fall time	1	2	0.3 toi	µs
tdrt	Delay time, R∅ stop to I∅ rising	5	60	(see note 20)	µs
tdtr	Delay time, I∅ falling to R∅ start	5	60	(see note 20)	µs
Trr	Register clock period (see note 21)	200	1333	(see note 20)	ns
tdrg	Delay time, R∅ falling to DG rising (see note 22)	5	20	N/A	µs
tdgr	Delay time, DG falling to R∅ rising (see note 22)	5	20	N/A	µs
trr	Register clock pulse rise time	10	50	(see note 20)	ns
Tfr	Register clock pulse fall time	10	50	(see note 20)	ns
tor	Register clock pulse edge overlap	10	50	(see note 20)	ns
twx	Reset pulse width (see note 21)	>2 trx	125	250	ns
trx	Reset pulse rise time	2	50	0.5 tWX	ns
tfx	Reset pulse fall time	2	50	0.5 tWX	ns

NOTES

18. Generally, $T_i = t_{drt} + 7t_{oi} + t_{dtr}$.
19. The R∅2 pulse-width is normally minimised, as shown, such that the R∅1 and R∅3 pulse widths can be increased to maximise the output reset (or reference) and signal sampling intervals.
20. As set by any system specifications.
21. The typical timing is for read-out at frequencies in the region of 750 kHz as per factory testing. Minimum period is that required for operation at 5 MHz but this is untested in the factory.
22. Dump gate not used in clocked mode for factory testing. Minimum and typical values are for guide only.

PACKAGE DETAIL

All dimensions shown in mm. Dimensions without limits are nominal. Contact Teledyne e2v for further package details.



HEALTH AND SAFETY HAZARDS

Teledyne e2v devices are safe to handle and operate, provided that the relevant precautions stated herein are observed. Teledyne e2v does not accept responsibility for damage or injury resulting from the use of devices it produces. Equipment manufacturers and users must ensure that adequate precautions are taken. Appropriate warning labels and notices must be provided on equipment incorporating Teledyne e2v devices and in operating manuals.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (i.e. all CCD pins except SS, DD, RD, OD and OS) but not to the other pins.

The devices are assembled in a clean room environment. Teledyne e2v recommend that similar precautions are taken to avoid contaminating the active surface.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to an ionising radiation. Users planning to use CCDs in a high radiation environment are advised to contact Teledyne e2v.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	143	-	373	K
Operating	153	-	323	K

Full performance is only guaranteed at the nominal operating temperature of 248 K.

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling ..... 5 K/min

PART REFERENCES

Variant	Illumination	Enhanced BSI Process	Silicon	AR Coating	Fringe Suppression
CCD230-84-G-145	BSI	No	Standard	Midband	No
CCD230-84-G-E04	BSI	No	Standard	Broadband	No
CCD230-84-G-E26	BSI	No	Standard	Uncoated	No

Grade Definitions

Grade 0	Super Grade	Meets all Grade 0 performance parameters and cosmetic parameters
Grade 1	Science Grade	Meets all Grade 1 performance parameters and cosmetic parameters
Grade 2	Low Science Grade	Meets all Grade 2 performance parameters and cosmetic parameters. Grade 2 have limited availability and offered on a case-by-case basis.
Grade 5	Engineering Grade	Electrically functional with no performance or cosmetic parameter guarantees
Grade 6	Mechanical Grade	Non-functional. Mechanically representative only.

NOTES

23.G = Grade (e.g. 1)
24.Additional variants may be available to custom order. Consult Teledyne e2v for more information.