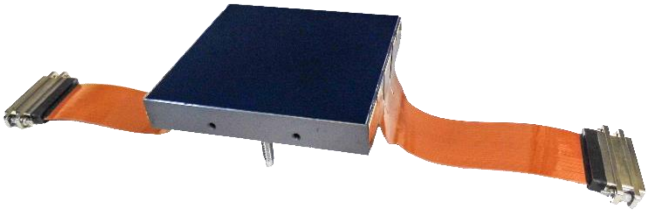
CCD290-99

85MP BSI CCD



KEY FEATURES

- 9216 x 9232 active pixels
- 10µm square pixels
- Full-frame or split full-frame
- Non-inverted mode operation
- Very low noise output amplifiers
- Tight flatness tolerance
- Buttable Silicon Carbide package
- Deep Depletion option for Red/NIR

TYPICAL APPLICATIONS

- Astronomy

PART REFERENCES

Please see last page for full list of available parts.

GENERAL DATA

Format	
Image Area	92.2 × 92.4 mm
Active Pixels	9216(H) x 9232(V)
Pixel Size	10 × 10 µm
Number of output amplifiers	16
Package	
Package size	98.5 x 93.7 mm
Connectors	Two 51-way micro-D
Focal plane height, above base	20.0 mm
Height Tolerance	±15 µm
Performance	
Output amplifier sensitivity	7.5 µV/e^-
Typical readout noise	4 e^- at 0.5 MHz 2.5 e^- at 50 kHz
Max output data rate	3 MHz
Typical pixel charge capacity	90 ke^-/pixel
Typical dark signal (-100°C)	4 e^-/pixel/hour
Typical flatness (peak to valley)	20 µm

OVERVIEW

The CCD290-99 is a large area CCD designed for high performance Astronomy applications. The Teledyne e2v back-thinning process ensures high quantum efficiency over a wide range of wavelengths.

The compact footprint package allows for 4-side butting of multiple CCDs into focal plane arrays

The image area has two separately connected sections to allow full-frame or split full-frame read-out modes. Depending on the mode, the read-out can be through 8 or 16 of the output circuits. A fixed-barrier dump drain is also provided to allow fast dumping of unwanted data.

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PERFORMANCE

Parameter		Grade 0 and 1			Grade 2			
		Typical	Min	Max	Min	Max	Units	Note
Peak charge storage (image)		90,000	70,000	-	60,000	-	e^-/pixel	2(a)
Peak charge storage (register/SW)	OG low (mode 1)	140,000	-	-	-	-	e^-/pixel	2(b)
Output node capacity	OG low (mode 1)	240,000	-	-	-	-	e^-	2(c)
	OG high (mode 2)	700,000	-	-	-	-	e^-	
Output amplifier responsivity	mode 1	7.5	5.5	-	5.0	-	µV/e^-	3
	mode 2	2.5	-	-	-	-	µV/e^-	
Non-linearity		0.5	-1.5	+1.5	-3.0	+3.0	%	
Readout noise	50 kHz	2.5	-	-	-	-	e^- rms	4
	0.5 MHz	4	-	7	-	10	e^- rms	
Dark signal	At 173 K (measured)	4	-	-	-	-	e^-/pixel/hr	5
	At 153 K (calculated)	0.02	-	2.0	-	4.0	e^-/pixel/hr	
Charge transfer efficiency	Parallel	99.9995	99.9990	-	99.9985	-	%	6
	Serial	99.9995	99.9990	-	99.9985	-	%	
Flatness peak-to-valley		20	-	30	-	50	µm	7
Focal plane package height		20	19.985	20.015	19.970	20.030	mm	7

NOTES

1. Device performance will be within the limits specified by “max” and “min” when operated at the recommended voltages supplied with the test data and when measured at a register clock frequency in the range 0.1 – 1.0 MHz. Acceptance tests are performed at 173 K and at a nominal 0.5 MHz pixel rate.
2. (a) Signal level at which resolution begins to degrade. Device is non-inverted (NIMO/non-MPP), for maximum full well.

   (b) The summing well capacity limits the charge in the register. The limiting value may change in mode 2 but is not tested.

   (c) The signal handled by the output node (for linear operation) varies with mode as shown. Values are inferred by design and not factory tested.
3. Under normal operation (mode 1), SW is operated as a summing well or clocked as R∅3. OG is biased at a low DC level.

   Alternatively (mode 2), SW may be operated as an output gate (and not therefore available for summing), biased at a low DC level, with OG raised to a high voltage (see note 12 later). This gives more charge-handling capacity (e.g. for higher level pixel binning). Charge transfer to the output now occurs as R∅2 goes low. In mode-2, the output noise will also increase by a factor of three. Mode-2 is not factory tested.
4. Measured with correlated double sampling at 0.5 MHz nominal (mode 1). Performance at 50 kHz is also indicated but not factory tested. Noise (as with all factory test images) is measured with differential readout, i.e. using the dummy output. The noise value reported is a single ended equivalent value with no dummy, by dividing by the √2 factor that arises from the differential subtraction. This way test system induced noise contribution is reduced.
5. Dark signal is typically measured at a device temperature of 173 K. It is a strong function of temperature and the typical average (background) dark signal at any temperature T (Kelvin) between 150 K and 300 K is given by:

   $Q_d/Q_{do} = 122T^3e^{-6400/T}$

   where Q_{do} is the dark current at 293 K.

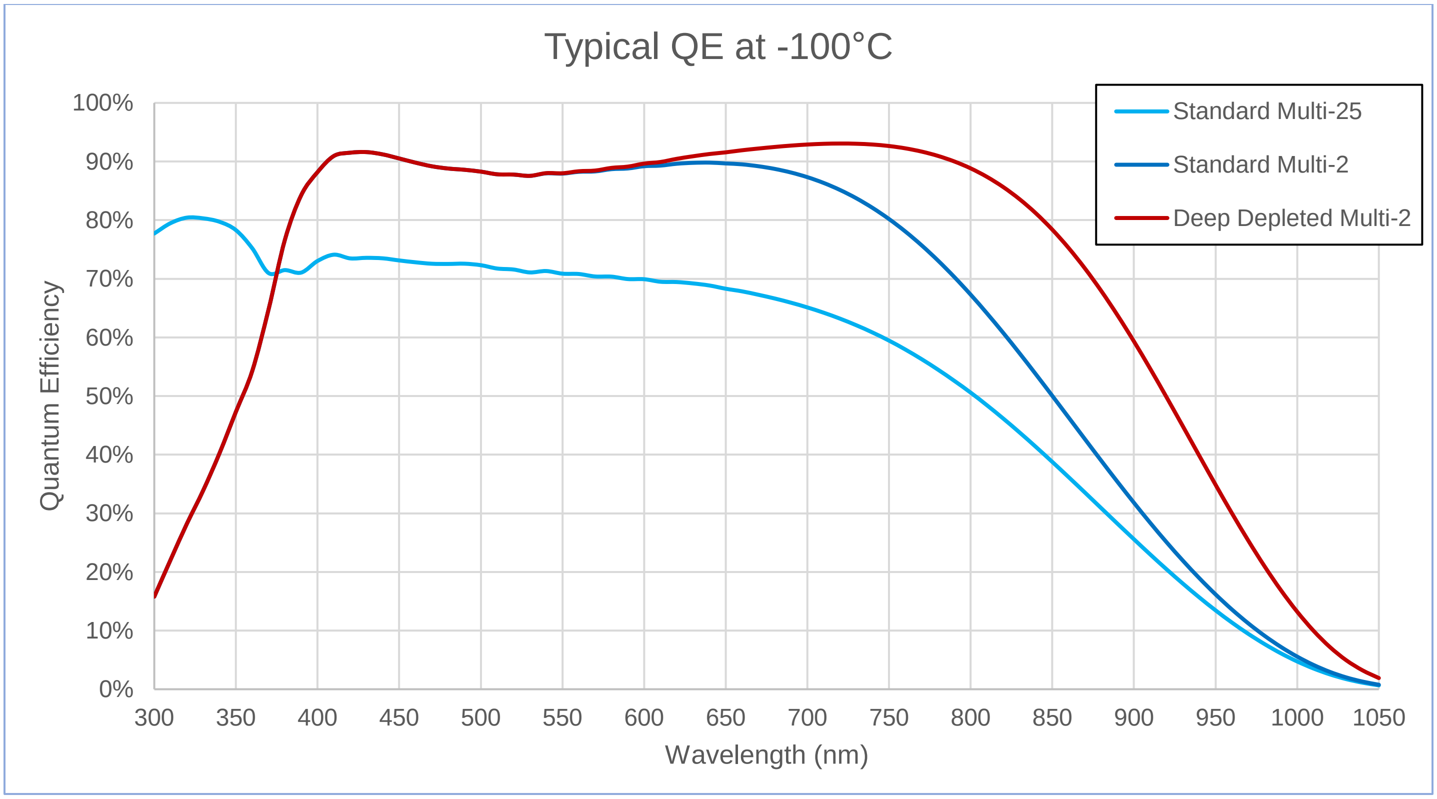
   Note that this is typical performance and some variation may be seen between devices.

6. Measured with a ^{55}Fe X-ray source. The CTE value is quoted for the complete clock cycle (i.e. not per phase).
7. Mechanical parameters are measured at room temperature. The flatness measured at room temperature is extrapolated to a value at 173 K based on modelling results.

SPECTRAL RESPONSE

The table below gives guaranteed minimum values of the spectral response for several variants with enhanced BSI process. Photo response non-uniformity (PRNU) is also shown. See also the typical spectral response figures below.

Wavelength (nm)	Minimum Response (QE)			Max PRNU (1 σ)	
	Standard Silicon		Deep Depleted Silicon		
	Multi-25	Multi-2	Multi-2		
300	65	-	-		
350	65	30	30	-	**%**
400	60	75	75	3	**%**
500	-	75	75	-	**%**
650	-	80	80	3	**%**
900	-	25	50	5	**%**



NOTES

8. The above specifications are for grade 0 and 1 devices. Grade 2 device specifications are 5% absolute lower for guaranteed QE minimum values and 1% absolute higher for guaranteed PRNU maximum values.
9. Standard silicon has a nominal active thickness of 16 µm. Deep Depleted silicon has a higher resistivity and a nominal active thickness of 40 µm.
10. Devices with alternative or custom spectral response may be available by special request. Consult Teledyne e2v

COSMETIC SPECIFICATIONS

Maximum allowed defect levels are indicated below. For cosmetic defect analysis, all image pixels are clocked to register E/F and read out using outputs OS1 to OS8 only.

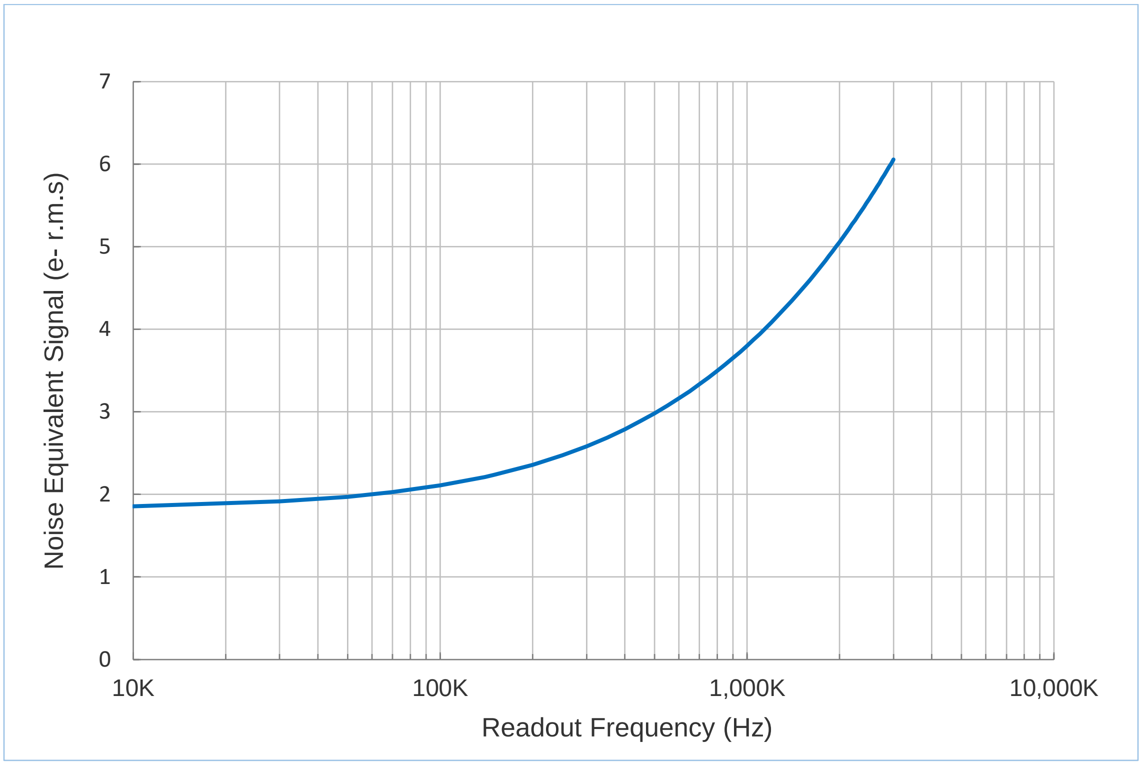
Standard and DD Silicon	**Guaranteed Specifications**			**Typical Values**		
Grade	**0**	**1**	**2**	**0**	**1**	**2**
Column defects - black or white	15	30	40	<5	<10	<20
White spots	1500	3000	4500	<1000	<2000	<3000
Total (black & white) spots	4000	8000	12000	<2000	<4000	<6000
Traps > 200e-	20	30	40	<10	<20	<30

Cosmetic definitions

White spots	A defect is counted as a white spot if the dark generation rate is ≥5 e^-/pixel/s at 173 K. (which is also equivalent to ≥100 e^-/hour at 153 K). The temperature dependence is the same as for the mean dark signal; see note 5 above.
Black spots	A black spot defect is a pixel with a photo-response less than 50% of the local mean.
Column defects	A column is counted as a defect if it contains at least 100 white or dark single pixel defects.
Traps	A trap causes charge to be temporarily held in a pixel and released in to following pixels during readout. With the sensor uniformly illuminated to a signal level of approximately 1000e-, a column is counted as having a trap if the quantity of trapped charge released in to the overscan pixels is greater than 200 e^-.
Defect exclusion zone	Defect measurements are excluded from the outer two rows and columns of the sensor.

AMPLIFIER READ NOISE

The theoretical variation of read noise with operating frequency is shown below. (If measured using correlated double sampling with a pre-sampling bandwidth equal to twice the pixel rate in mode 1, temperature range 150 – 230 K).



DEFINITIONS

Back-thinning

A back-thinned CCD is fabricated on the front surface of the silicon and is subsequently processed for illumination from the reverse side. This avoids loss of transmission in the electrode layer (particularly significant at shorter wavelengths or with low energy X-rays). This process requires the silicon to be reduced to a thin layer by a combination of chemical and mechanical means. The surface is “passivated” and an anti-reflection coating may be added.

AR Coating

Anti-reflection coatings are normally applied to the back illuminated CCD to further improve the quantum efficiency. Standard coatings optimise the response in the visible, ultra-violet or infrared regions. For X-ray detection an uncoated device may be preferable.

Readout Noise

Readout noise is the random noise from the CCD output stage in the absence of signal. This noise introduces a random fluctuation in the output voltage that is superimposed on the detected signal.

The method of measurement involves reverse-clocking the register and determining the standard deviation of the output fluctuations, and then converting the result to an equivalent number of electrons using the known amplifier responsivity.

Dummy Output

Each output has an associated “dummy” circuit on-chip, which is of identical design to the “real” circuit but receives no signal charge. The dummy output should have the same levels of clock feed-through and can thus be used to suppress the similar component in the “real” signal output by means of a differential pre-amplifier. The penalty is that the noise is increased by a factor of $\sqrt{2}$. If not required, the dummy outputs may be powered down.

Dark Signal

This is the output signal of the device with zero illumination. This typically consists of thermally generated electrons within the semiconductor material, which are accumulated during signal integration. Dark signal is a strong function of temperature as described in note 5.

Correlated Double Sampling

A technique for reducing the noise associated with the charge detection process by subtracting a first output sample taken just after reset from a second sample taken with charge present.

Charge Transfer Efficiency

The fraction of charge stored in a CCD element that is transferred to the adjacent element by a single clock cycle. The charge not transferred remains in the original element, possibly in trapping states and may possibly be released into later elements. The value of CTE is not constant but varies with signal size, temperature, and clock frequency.

ARCHITECTURE

Chip Schematic

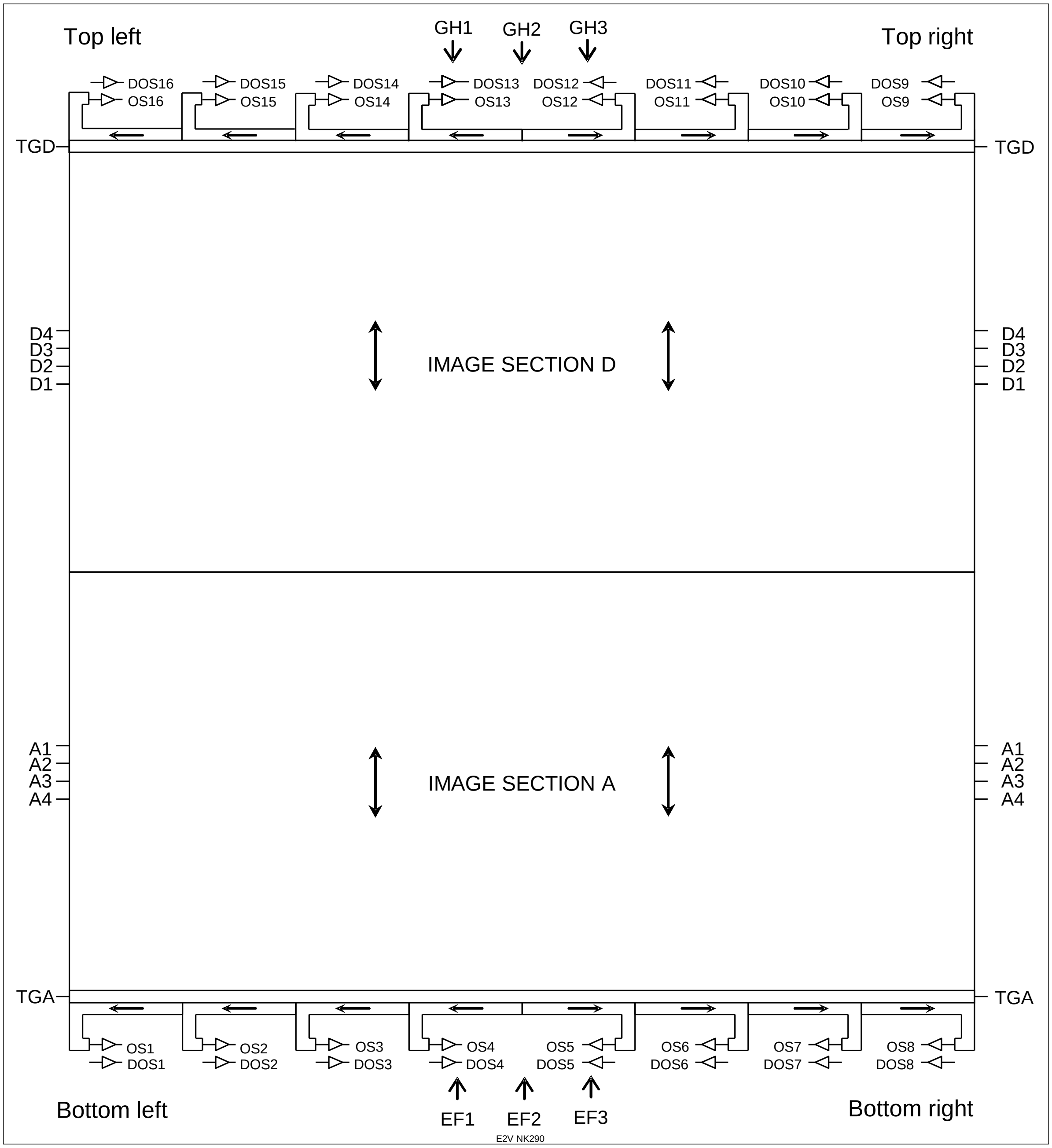
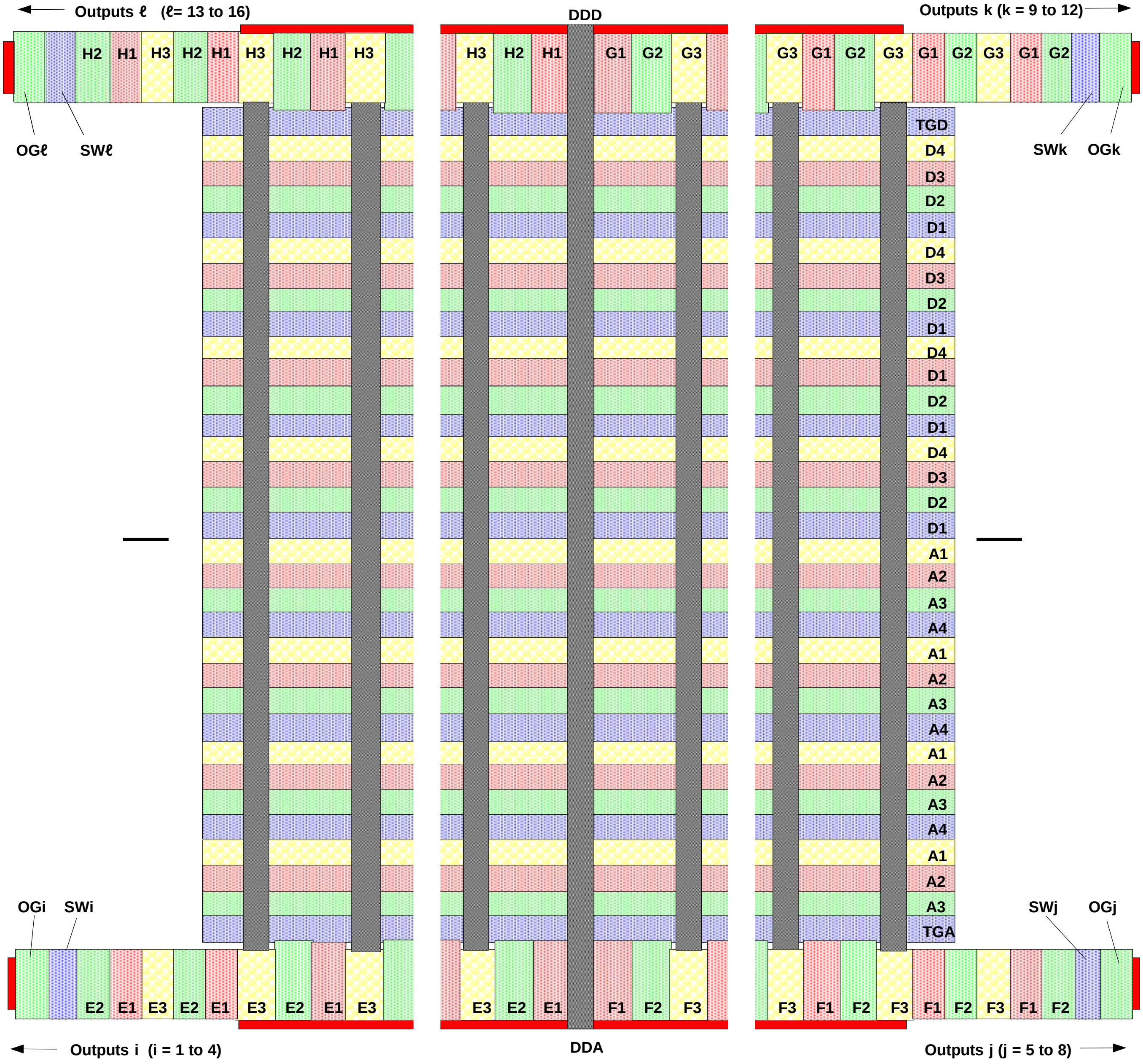


Image sections A and D each have a total of 9216 (H) × 4616 (V) pixels.

Each register section has a total of 1179 elements: 1152 active and 27 pre-scan.

Connector-1 (and flexi) is at the “bottom” of the device (register EF); Connector-2 is at the “top” of the device (register GH).

ARRANGEMENT OF ELECTRODES

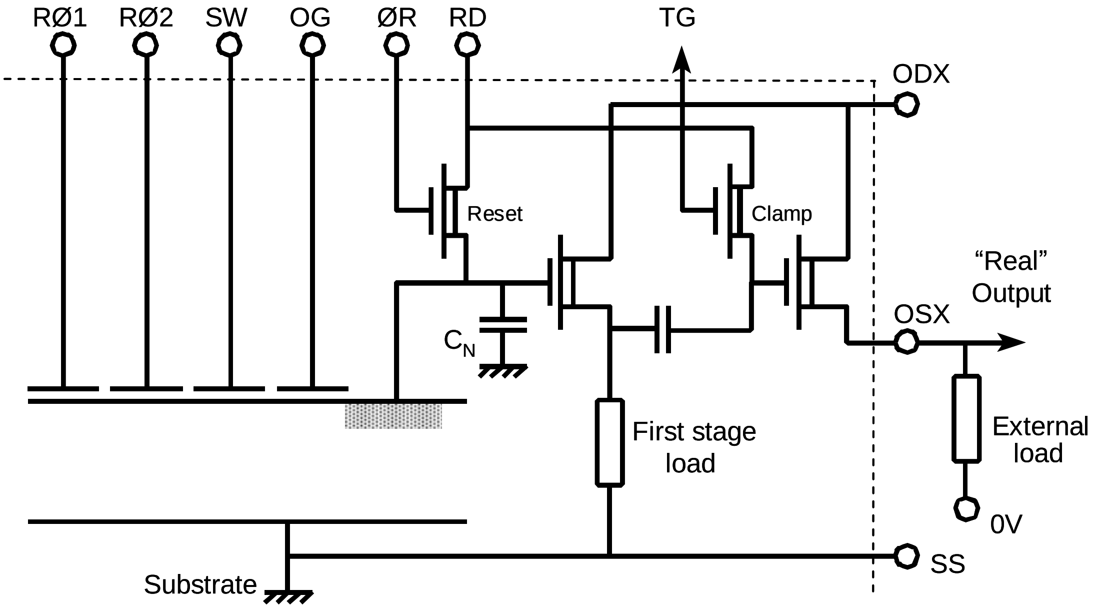


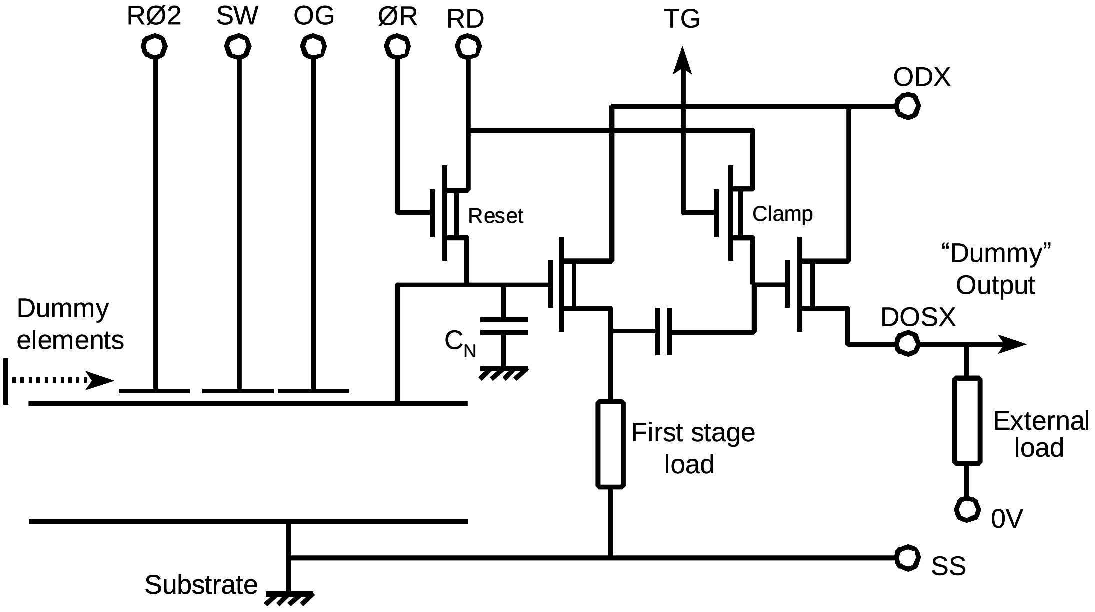
Pre-scan (blank) serial elements are not shown here.

Each output consists of real (OS) and dummy (DOS); see next page.

OUTPUT CIRCUIT

X designates a specific output, namely 1 to 16 (see the chip schematic).





The first stage load of each output (real or dummy) draws a quiescent current of approximately 0.2 mA via SS.

The output circuit consists of two capacitor-coupled source-follower stages. The particular design has a very high responsivity to give lowest noise. The load for the first stage is on-chip and that for the second stage is external, as next described. The DC restoration circuitry requires a pulse at the start of line readout, and this is automatically obtained by an internal connection to the adjacent transfer gate, TG. Transferring a line of charges to the register thus automatically activates the circuitry. TG pulses still need to be applied at similar intervals if only the register and/or output circuit are being operated, e.g. for test or characterisation purposes.

The amplifier output impedance is typically 400 Ω.

ELECTRICAL INTERFACE

CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

Note that the hyphenated suffix symbols (e.g. ∅R-E) indicate to which output any register or amplifier pin relates.

Flex Connector 1

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 12)			MAX RATINGS with respect to V_{SS} (V)
			Min	Typical	Max	
1	A1	Image Area A Clock Phase 1	9	11	12	±20
2	A2	Image Area A Clock Phase 2	9	11	12	N/A
3	TGA	Image Area A Transfer gate	9	11	12	N/A
4	OD1	Output Drain 1	25	29	31	-0.3 to +35
5	OS1	Output Source 1	(see note 11)			
6	OD2	Output Drain 2	25	29	31	-0.3 to +35
7	OS2	Output Source 2	(see note 11)			
8	OD3	Output Drain 3	25	29	31	-0.3 to +35
9	OS3	Output Source 3	(see note 11)			
10	OD4	Output Drain 4	25	29	31	-0.3 to +35
11	OS4	Output Source 4	(see note 11)			
12	SS	Substrate (see note 14)	0	0	10	N/A
13	ØRA	Reset Gate (A) (See note 15)	9	12	13	±20
14	SWA	Summing Well (A) (See note 12)	9	10	12	±20
15	SS	Substrate (see note 14)	0	0	10	N/A
16	OS5	Output Source 5	(see note 11)			
17	OD5	Output Drain 5	25	29	31	N/A
18	OS6	Output Source 6	(see note 11)			N/A
19	OD6	Output Drain 6	25	29	31	-0.3 to +35
20	OS7	Output Source 7	(see note 11)			
21	OD7	Output Drain 7	25	29	31	-0.3 to +35
22	OS8	Output Source 8	(see note 11)			
23	OD8	Output Drain 8	25	29	31	-0.3 to +35
24	TGA	Image Area A Transfer Gate	9	11	12	±20
25	A2	Image Area A Clock Phase 2	9	11	12	±20
26	A1	Image Area A Clock Phase 1	9	11	12	±20
27	A3	Image Area A Clock Phase 3	9	11	12	±20
28	A4	Image Area A Clock Phase 4	9	11	12	±20
29	RD1/2	Reset Drain (1/2)	16	17	19	-0.3 to +25
30	DOS1	Dummy Output Source 1	(see note 11)			
31	SS	Substrate (see note 14)	0	0	10	N/A
32	DOS2	Dummy Output Source 2	(see note 11)			
33	RD 3/4	Reset Drain (3/4)	16	17	19	-0.3 to +25
34	DOS3	Dummy Output Source 3	(see note 11)			
35	SS	Substrate (see note 14)	0	0	10	N/A
36	DOS4	Dummy Output Source 4	(see note 11)			
37	OGA	Output Gate (A) (See note 12)	1	2	(note 12)	±20
38	E3/F3	Register E & Register F Clock Phase 3	9	10	12	±20
39	E2/F2	Register E & Register F Clock Phase 2	9	10	12	±20
40	E1/F1	Register E & Register F Clock Phase 1	9	10	12	±20
41	DDA	Dump Drain (A) (See note 16)	15	18	20	-0.3 to +35
42	DOS5	Dummy Output Source 5	(see note 11)			
43	SS	Substrate (see note 14)	0	0	10	N/A
44	DOS6	Dummy Output Source 6	(see note 11)			
45	RD5/6	Reset Drain (5/6)	16	17	19	-0.3 to +25
46	DOS7	Dummy Output Source 7	(see note 11)			
47	SS	Substrate (see note 14)	0	0	10	N/A
48	DOS8	Dummy Output Source 8	(see note 11)			
49	RD7/8	Reset Drain (7/8)	16	17	19	-0.3 to +25
50	A4	Image Area A Clock Phase 4	9	11	12	±20
51	A3	Image Area A Clock Phase 3	9	11	12	±20

Flex Connector 2

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 12)			MAX RATINGS with respect to V_{SS} (V)
			Min	Typical	Max	
1	A1	Image Area A Clock Phase 1	9	11	12	±20
2	A2	Image Area A Clock Phase 2	9	11	12	N/A
3	TGA	Image Area A Transfer gate	9	11	12	N/A
4	OD1	Output Drain 1	25	29	31	-0.3 to +35
5	OS1	Output Source 1	(see note 11)			
6	OD2	Output Drain 2	25	29	31	-0.3 to +35
7	OS2	Output Source 2	(see note 11)			
8	OD3	Output Drain 3	25	29	31	-0.3 to +35
9	OS3	Output Source 3	(see note 11)			
10	OD4	Output Drain 4	25	29	31	-0.3 to +35
11	OS4	Output Source 4	(see note 11)			
12	SS	Substrate (see note 14)	0	0	10	N/A
13	ØRA	Reset Gate (A) (See note 15)	9	12	13	±20
14	SWA	Summing Well (A) (See note 12)	9	10	12	±20
15	SS	Substrate (see note 14)	0	0	10	N/A
16	OS5	Output Source 5	(see note 11)			
17	OD5	Output Drain 5	25	29	31	N/A
18	OS6	Output Source 6	(see note 11)			N/A
19	OD6	Output Drain 6	25	29	31	-0.3 to +35
20	OS7	Output Source 7	(see note 11)			
21	OD7	Output Drain 7	25	29	31	-0.3 to +35
22	OS8	Output Source 8	(see note 11)			
23	OD8	Output Drain 8	25	29	31	-0.3 to +35
24	TGA	Image Area A Transfer Gate	9	11	12	±20
25	A2	Image Area A Clock Phase 2	9	11	12	±20
26	A1	Image Area A Clock Phase 1	9	11	12	±20
27	A3	Image Area A Clock Phase 3	9	11	12	±20
28	A4	Image Area A Clock Phase 4	9	11	12	±20
29	RD1/2	Reset Drain (1/2)	16	17	19	-0.3 to +25
30	DOS1	Dummy Output Source 1	(see note 11)			
31	SS	Substrate (see note 14)	0	0	10	N/A
32	DOS2	Dummy Output Source 2	(see note 11)			
33	RD 3/4	Reset Drain (3/4)	16	17	19	-0.3 to +25
34	DOS3	Dummy Output Source 3	(see note 11)			
35	SS	Substrate (see note 14)	0	0	10	N/A
36	DOS4	Dummy Output Source 4	(see note 11)			
37	OGA	Output Gate (A) (See note 12)	1	2	(note 12)	±20
38	E3/F3	Register E & Register F Clock Phase 3	9	10	12	±20
39	E2/F2	Register E & Register F Clock Phase 2	9	10	12	±20
40	E1/F1	Register E & Register F Clock Phase 1	9	10	12	±20
41	DDA	Dump Drain (A) (See note 16)	15	18	20	-0.3 to +35
42	DOS5	Dummy Output Source 5	(see note 11)			
43	SS	Substrate (see note 14)	0	0	10	N/A
44	DOS6	Dummy Output Source 6	(see note 11)			
45	RD5/6	Reset Drain (5/6)	16	17	19	-0.3 to +25
46	DOS7	Dummy Output Source 7	(see note 11)			
47	SS	Substrate (see note 14)	0	0	10	N/A
48	DOS8	Dummy Output Source 8	(see note 11)			
49	RD7/8	Reset Drain (7/8)	16	17	19	-0.3 to +25
50	A4	Image Area A Clock Phase 4	9	11	12	±20
51	A3	Image Area A Clock Phase 3	9	11	12	±20

NOTES

11. Do not connect to voltage supply but use a ~5 mA current source or a ~5 kΩ external load. The quiescent voltage on OS is then about 6 - 8 V above the reset drain voltage and is typically 24 V. The current through these pins must not exceed 20 mA. Permanent damage may result if, in operation, OS or DOS experience short circuit conditions.

    For highest speed operation the output load resistor can be reduced from 5 kΩ to approximately 2.2 kΩ, but note that this will increase power consumption. If the device is to be operated with a register clock period of below about 1 MHz then the load may be increased to 10 kΩ to reduce power consumption.

12. Default operation (mode 1) shown with OG set to OG-Low, with a +2 V nominal value. In this mode SW may be clocked as RØ3 if a summing well function is not required. OG-Low should have a maximum value of +5 V.

    For alternative operation in a low responsivity mode (mode 2) with increased charge handling, OG should be set to OG-High and SW should be operated as OG-Low (i.e. 2V typical). See below for appropriate OG-High values. Charge is now read out as RØ2 goes low.

    See note 14 also for discussion about Substrate voltage (Vss). With high substrate voltage OG-High may be set to a nominal +20 V, which offers best linearity in mode-2. With low substrate voltage, the allowed maximum value of OG-High is limited to a nominal +18 V; the lower OG-High value has a greater non-linearity.

13. To ensure that any device can be operated the camera should be designed so that any value in the range “min” to “max” can be provided. All operating voltages are with respect to image clock low (nominally 0 V).

    For the clock pulses, the high levels are shown in the table. The image clock low is set to 0 V . The register and SW clock low levels are +1 V. Reset clock low is set to 0 V.

    In all cases, specific recommended settings will be supplied with each science-grade sensor.Non-charge dumping level shown. For charge dumping, DG should be pulsed to 12 ± 2 V.

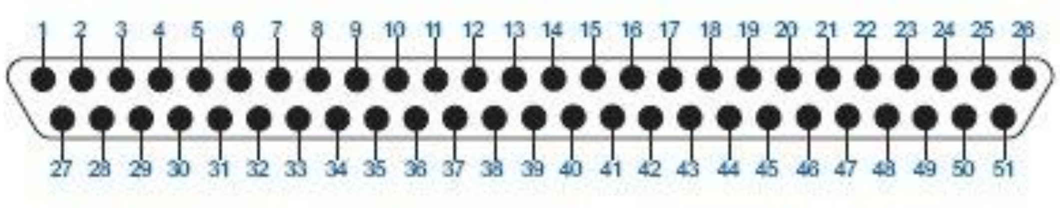
14. The substrate voltage (Vss) has a default value of 0 V (“low” substrate). This is particularly recommended for deep-depletion device variants, since it optimises depletion depth for best Point Spread Function. Devices may alternatively be operated at “high” substrate, with Vss = 9 V. The high substrate setting offers slightly lower dark current, although this is usually not of primary concern when the device is cryogenically cooled. See also note 22 below, referring to Vss level as prior to readout.

    The substrate setting has some consequence for the allowed OG upper voltage level, as discussed in note 12. Standard silicon variants are expected to be used with ∅R at +10 V or more; deep depletion variants require at least +12 V. A higher value will give a correspondingly higher reset feedthrough signal in the device output (OS).

15. Standard silicon variants are expected to be used with ØR at +10 V or more; deep depletion variants require at least +12 V. A higher value will give a correspondingly higher reset feed-through signal in the device output (OS).

16. The DD function may change in future versions. Consult factory for information. The DD voltage level determines the level at which register overspill into the drain occurs.

PIN CONNECTIONS (View facing pins of connector)



This numbering applies to all connectors. The connector is a Glenair 51P micro D type.

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (defined at mid-clock level)

	Typical	Units
IØ/IØ inter-phase [A, D]	70	nF
IØ/SS per phase [A, D]	20	nF
Total IØ per phase (to Vss and two inter-phase)	160	nF
Transfer gates [TGA, TGD]	150	pF
RØ total per phase [each of E1/F1, G1/H1]	450	pF
RØ total per phase [each of E2/F2, G2/H2]	600	pF
RØ total per phase [each of E3/F3, G3/H3]	650	pF

The total capacitance to be driven per phase is the sum of the component to substrate and the inter-phase components to each of the adjacent phases. With 8 images phases the total parallel capacitance is 1.28 □F. Summing each of the 6 register phase capacitances gives a total serial capacitance of 3.4 nF.

POWER UP/POWER DOWN

When powering the device up or down it is critical that any specified maximum rating is not exceeded. Specifically the voltages for the amplifier and dump drains (OD, RD, DD) must never be taken negative with respect to the substrate. Hence, if the substrate is to be operated at a positive voltage (e.g. to minimise dark current) then the drive electronics should have a switch-on sequence which powers up all the drains to their positive voltages before the substrate voltage starts to increase from zero.

It is also important to ensure that excess currents (see note 11) do not flow in the OS or DOS pins. Such currents could arise from rapid charging of a signal coupling capacitor or from an incorrectly biased DC-coupled preamplifier.

Similarly, for powering down, the substrate must be taken to zero voltage before the drains.

POWER CONSUMPTION

The power dissipated within the CCD is a combination of the static dissipation of the amplifiers and the dynamic dissipation from both of the parallel and serial clocking (i.e. driving the capacitive loads). The dynamic power dissipation (P) is determined separately for the serial and parallel clocking using capacitance, voltage and frequency values via the P = CV2f relationship. This will be the total clocked power and is divided between the drive buffer (off-chip) and the device (on-chip).

The table below gives representative values for the components of the on-chip power dissipation for the case of continuous split-frame line-by-line readout using both registers and all the output circuits with both real and dummy amplifiers activated. The frequency is that for clocking the serial register and an appropriate value of the amplifier load is utilised in each case.

Readout frequency	Line time	Amplifier load	Power dissipation			
			Amplifiers	Serial clocks	Parallel clocks	Total
0.5 MHz	12.3 s	2.7 ms	5 kΩ	800 mW	~138 mW	~ 58 mW
1 MHz	6.8 s	1.5 ms	5 kΩ	800 mW	~275 mW	~105 mW
3 MHz	3.2 s	0.7 ms	5 kΩ	800 mW	~826 mW	~ 223 mW

Line transfer time and clock amplitudes are taken as the typical values listed in the clock timing requirements and electrical interfaces tables. 1179 register pixels are readout per register section for a total of 4616 rows.

The dissipation reduces to only that of the amplifiers during the time that charge is being collected in the image sections with both the parallel and serial clocks static.

Each flex-cable has a thermal conductivity of approximately 1 mW/°C.

FRAME READOUT MODES

The device can be operated in a full-frame or split full-frame mode.

If the applied drive pulses are designated IØ1, IØ2, IØ3 and IØ4, then connections should be made as tabulated below to effect the following directions of transfer.

Clock Generator Drive Pulse Name	IØ1	IØ2	IØ3	IØ4	
A section transfer towards E register	A1	A2	A3	A4	TGA = IØ4
D section transfer towards G register	D1	D2	D3	D4	TGD = IØ1
A section transfer towards G register	A4	A3	A2	A1	TGA = “low”
D section transfer towards E register	D4	D3	D2	D1	TGD = “low”

The first two transfer sequences are for split frame read-out. The second two are for reversing the transfer direction in either section for read-out to either the top or the bottom register sections.

Transfer from the image section to the register is into the phase 1 and 2 electrodes, i.e. E/F1, G/H1, E/F2 and G/H2. These electrodes must be held at clock “high” level during the process. If the register pulses are designated RØ1, RØ2 and RØ3, then connections should be made as tabulated below.

Clock Generator Drive Pulse Name	RØ1	RØ2	RØ3
E section	E1/F1	E2/F2	E3/F3
G section	G1/H1	G2/H2	G3/H3

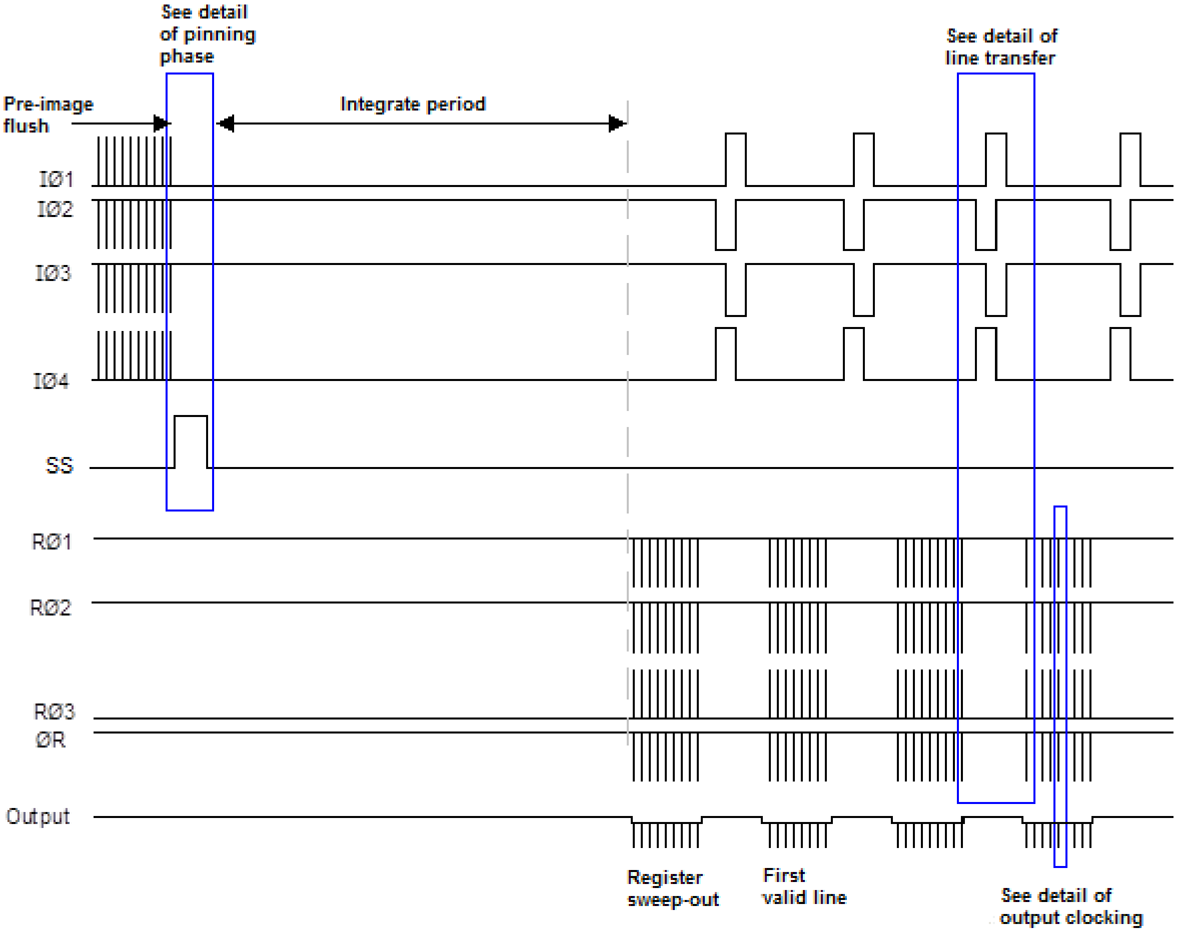
The last electrode before the output gate is separately connected to give the function of a summing well (SW). In normal readout (i.e. if not used for summing), SW is clocked as RØ3. For summing, the selected SW gate is held at clock “high” level for the required number of readout cycles, and then clocked as RØ3 to output charge.

Alternatively, SW may be operated as a second output gate to provide the option of operation in low gain/high signal mode (mode 2) with OG high. If this mode of operation is used, then the sequencing of the output clocks must be changed, as charge now transfers into the output node as RØ2 goes low (see note 12 above also).

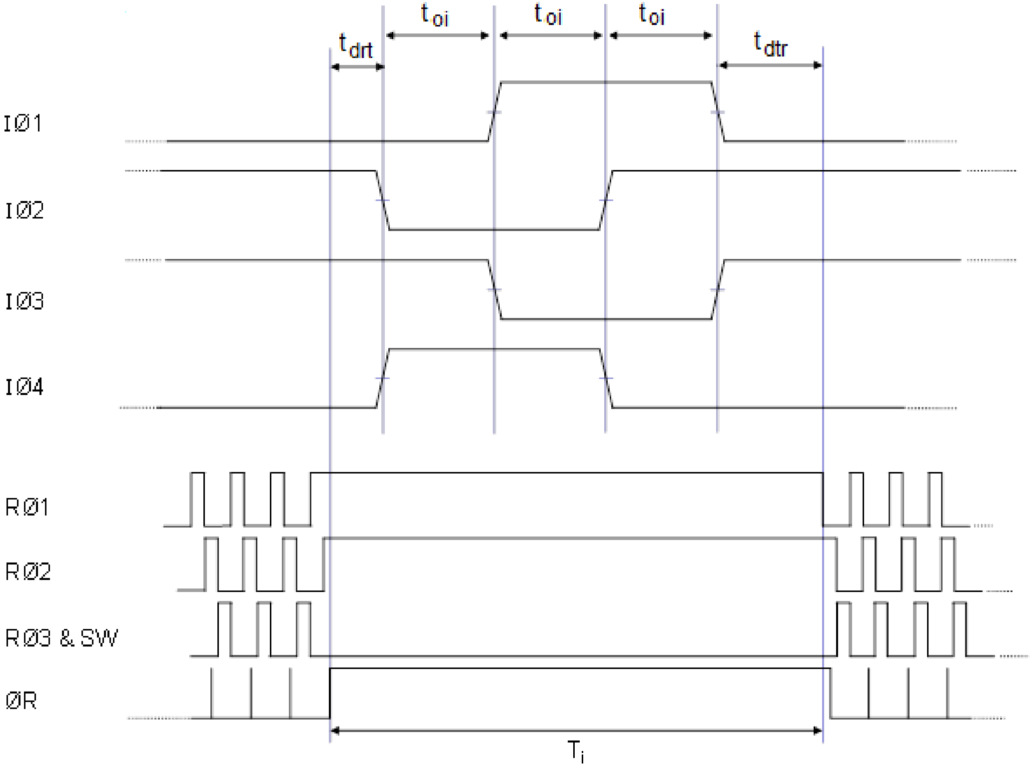
Image phases 2 and 3 should be held high during signal collection, as shown in the following figures.

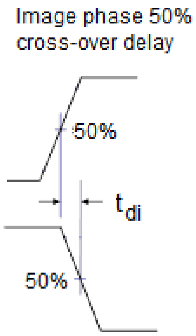
The register is provided with an anti-blooming dump drain to limit the peak signal capacity. For charge dumping purposes rows of charge signals may be clocked into the register sections and any excess charge above full-well capacity spills into the drain. There must then be a single line read-out to remove the unwanted charge (i.e. which can be up to the full-well capacity) before transferring the wanted row or rows of charge signals into the register sections. However, please see note 16 above also.

FRAME READOUT TIMING DIAGRAM

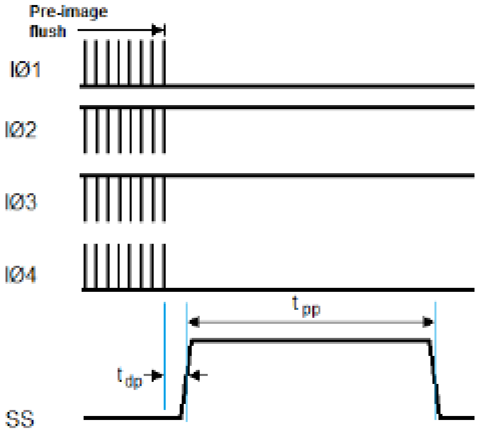


DETAIL OF LINE TRANSFER

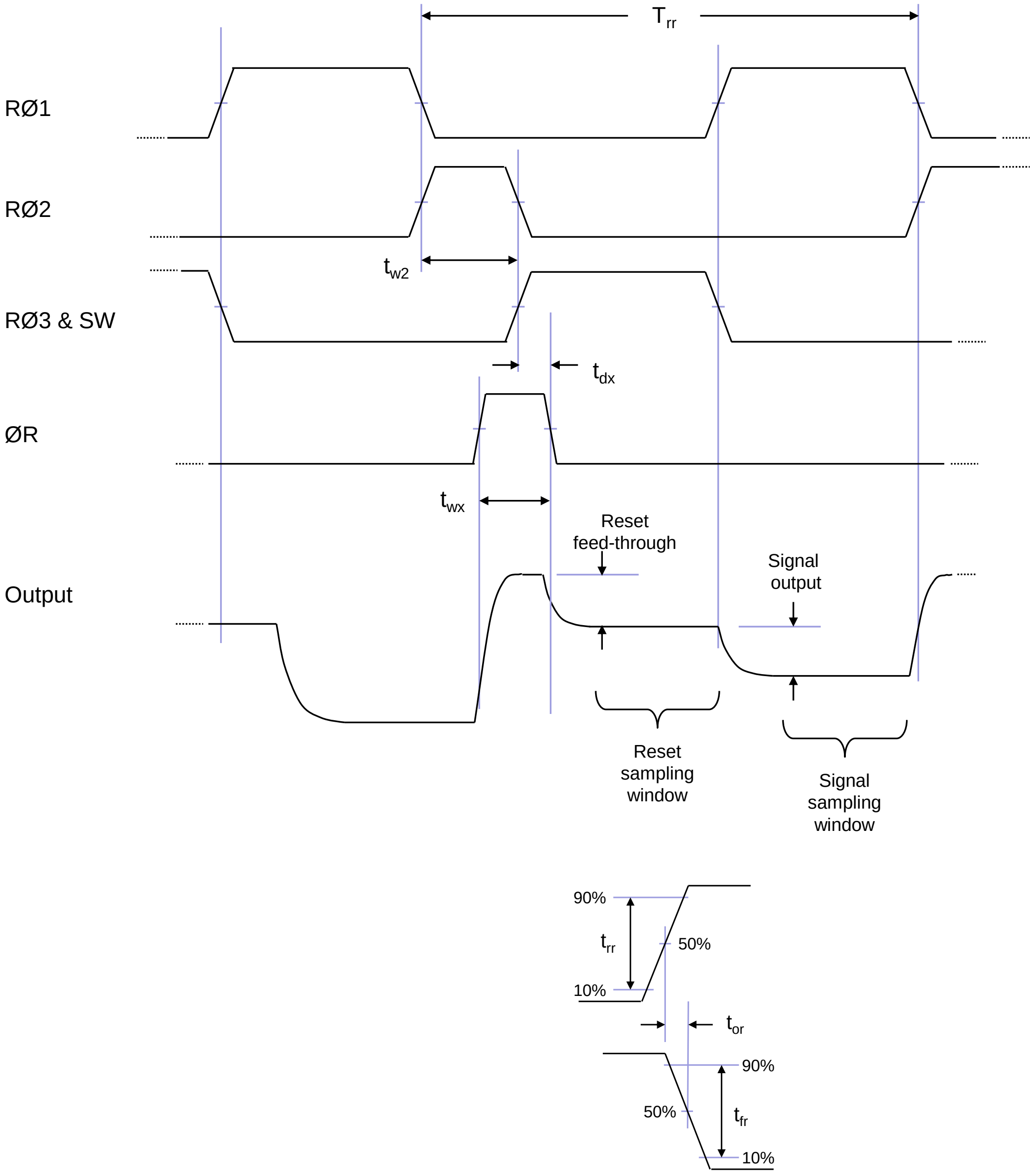




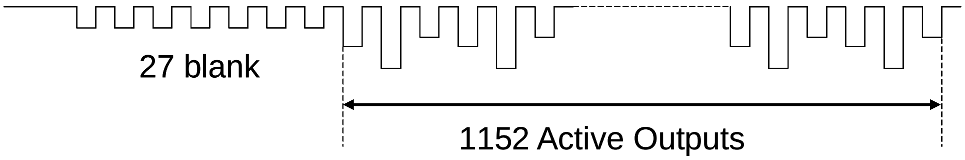
DETAIL OF PINNING PHASE (see note 22)



DETAIL OF OUTPUT CLOCKING (with SW clocked as RØ3)



LINE OUTPUT FORMAT



CLOCK TIMING REQUIREMENTS

Symbol	Description	Minimum	Typical	Maximum	Units
Ti	Line transfer time (see note 17)	120	300	-	µs
tdi	Delay in falling image clock 50 % point from rising image clock 50 %point (see note 18)	0	30	500	ns
toi	Image clock pulse overlap	25	60	-	µs
tri	Image clock and transfer gate pulse rise time	2	5	0.3 toi	µs
tfi	Image clock and transfer gate pulse fall time	2	5	0.3 toi	µs
tdrt	Delay time, RØ stop to IØ rising	15	30	-	µs
tdtr	Delay time, IØ falling to RØ start	30	80	-	µs
tpp	Substrate high duration during pinning phase	150	150	-	ms
tdp	Delay time, last image flush clock transition to to substrate rising	3	3	-	ms
Trr	Register clock period (see note 19)	300	2000	(see note 20)	ns
tw2	RØ2 pulse width at 50% levels (see note 21)	3trx	350	Trr/3	ns
trr	Register clock pulse rise time	10	70	0.05Trr	ns
tfr	Register clock pulse fall time	10	70	0.05Trr	ns
tor	Register clock pulse edge overlap at 50% levels	0	50	0.05Trr	ns
twx	Reset pulse width at 50% levels	3trx	300	0.2Trr	ns
trx	Reset pulse rise time	10	50	0.2twx	ns
tfx	Reset pulse fall time	10	50	0.2twx	ns
tdx	Delay time, RØ falling to ØR falling	2tfr	150	-	ns

NOTES

17. $T_i = t_{drt} + 3t_{oi} + t_{dtr}$.

18. The IØ1/IØ3, IØ2/IØ4, IØ3/IØ1 and IØ4/IØ2 transitions are nominally coincident with the edges overlapping at 50% amplitude.

19. The typical timing is for readout at frequencies in the region of 500 kHz, as used for factory testing.

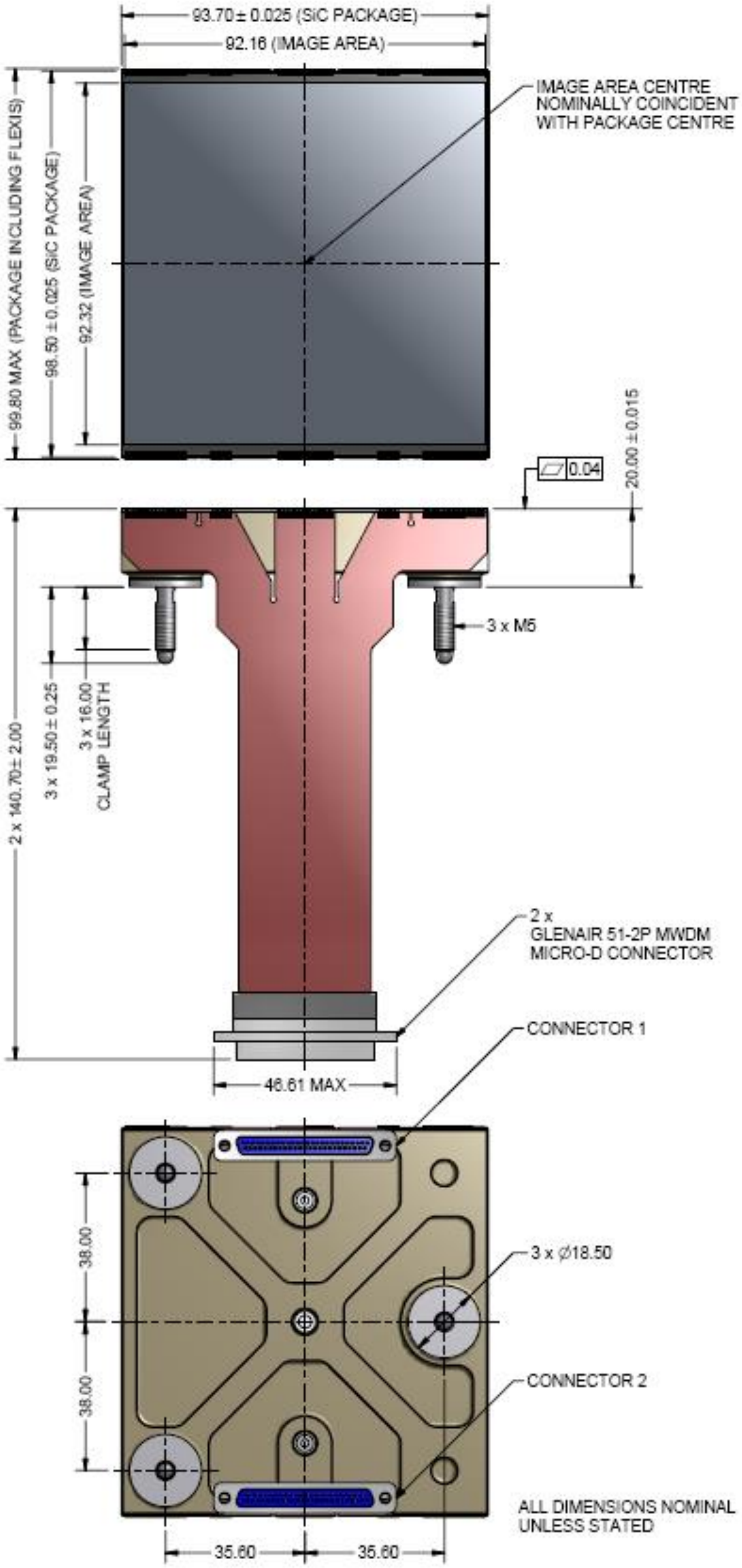
20. For highest speed operation the output load resistor can be reduced from 5 kΩ to approximately 2.2 kΩ, but note that this will increase power consumption. If the device is to be operated with a register clock period of below about 1 MHz, then the load may be increased to 10 kΩ to reduce power consumption.

21. The RØ2 pulse-width is normally minimised, as shown, such that the RØ1 and RØ3 pulse widths can be increased to maximise the output reset and signal sampling intervals.

22. The large area and small pixel size of the CCD290 requires changes to be made to the standard mode of operation, particularly for devices manufactured from deep depletion silicon. This is because for this version of the CCD290, holes are not efficiently removed from the device with standard clocking and it is possible that the structure can be left with holes partially filling the isolation regions giving a photo-response non uniformity along each column. Visually this appears as a “tear” in the image. This effect is most visible with flat field images and is independent of image intensity. To remove this effect the substrate should be pulsed high by +10 V with respect to image clock low for a short period prior to integration, This substrate high pinning phase is implemented by e2v during acceptance testing. Alternatively, the image clocks can be reduced -10V below substrate if independent control of substrate voltage is not available.

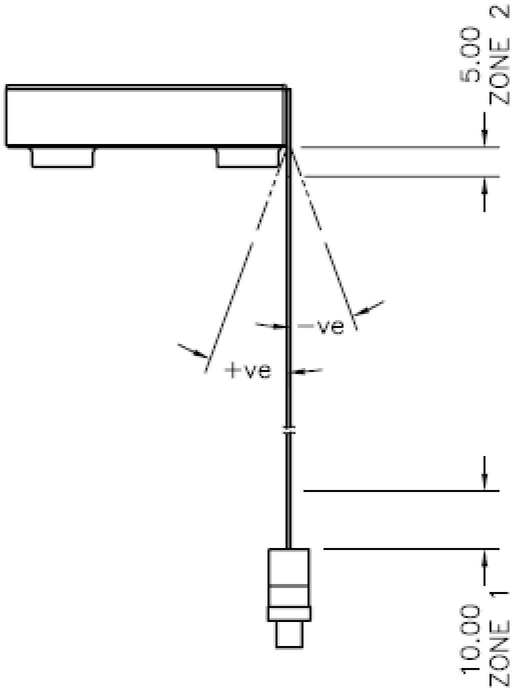
PACKAGE DETAIL

All dimensions shown in mm. Dimensions without limits are nominal. Contact Teledyne e2v for further package details.



The package base is Silicon Carbide; fitted with two flex-cable connectors and three mounting studs.

Interface drawing DAS772494AT (available on request) provides further information



The bend radius of the flexi PCB is recommended to be no less than 10 mm, with an absolute minimum of 5.8 mm. There should be no forced bending within 10mm of the connector potting (zone 1). There should be no forced bending of the flexi in the negative direction within 5 mm of the flexi to package bondline (zone 2).

HEALTH AND SAFETY HAZARDS

Teledyne e2v devices are safe to handle and operate, provided that the relevant precautions stated herein are observed. Teledyne e2v does not accept responsibility for damage or injury resulting from the use of devices it produces. Equipment manufacturers and users must ensure that adequate precautions are taken. Appropriate warning labels and notices must be provided on equipment incorporating Teledyne e2v devices and in operating manuals.

HANDLING CCD SENSORS

CCD sensors, in common with most high-performance MOS IC devices, are static sensitive. In certain cases, a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Should not be left unattended with pins floating and pins should be shorted together

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (i.e. all CCD pins except SS, DD, RD, OD and OS) but not to the other pins.

The devices are assembled in a clean room environment. Teledyne e2v recommend that similar precautions are taken to avoid contaminating the active surface.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to an ionising radiation. Users planning to use CCDs in a high radiation environment are advised to contact Teledyne e2v.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	148	-	358	K
Operating	153	-	323	K

Performance parameters are measured with the device at a temperature of 173 K and, as a result, full performance is only guaranteed at this nominal operating temperature.

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling............. 5 K/min

PART REFERENCES

Variant	Package	Illumination	Enhanced BSI Process	Silicon	AR Coating	Fringe Suppression
CCD290-99-G-H90	SiC Buttable	BSI	Yes	Standard	Multi-25	No
CCD290-99-G-F82	SiC Buttable	BSI	Yes	Standard	Multi-2	No
CCD290-99-G-F24	SiC Buttable	BSI	Yes	Deep Depletion	Multi-2	No

Grade Definitions

Grade 0	Super Grade	Meets all Grade 0 performance parameters and cosmetic parameters
Grade 1	Science Grade	Meets all Grade 1 performance parameters and cosmetic parameters
Grade 2	Low Science Grade	Meets all Grade 2 performance parameters and cosmetic parameters. Grade 2 have limited availability and offered on a case-by-case basis.
Grade 5	Engineering Grade	Electrically functional with no performance or cosmetic parameter guarantees
Grade 6	Mechanical Grade	Non-functional. Mechanically representative only.

NOTES

23. G = Grade (e.g. 1)
24. Additional variants may be available to custom order. Consult Teledyne e2v for more information.