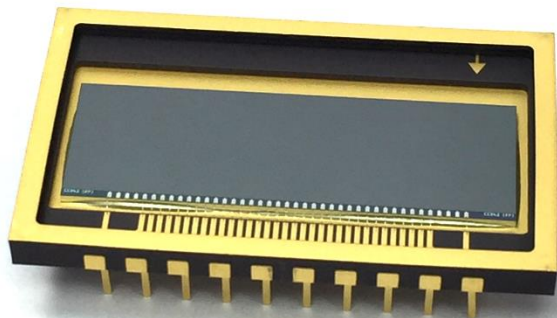


CCD42-10

2048 x 512 BSI CCD Sensor



KEY FEATURES

- 2048 x 512 active pixels
- 13.5µm square pixels
- Back Illuminated
- Wide Dynamic Range
- Advanced inverted mode operation
- Symmetrical anti-static gate protection

TYPICAL APPLICATIONS

- Spectroscopy
- Scientific Imaging
- TDI Operation

PART REFERENCES

Please see last page for full list of available parts.

GENERAL DATA

Format	
Image Area	27.6 × 6.9 mm
Active Pixels	2048(H) × 512(V)
Pixel Size	13.5 × 13.5 µm
Number of output amplifiers	2
Package	
Package Size	32.89 x 20.07 mm
Number of Pins	20
Inter-pin Spacing	2.54 mm
Window Material	Removable Glass
Package Type	Ceramic DIL array
Performance	
Maximum readout frequency	3 MHz
Output amplifier sensitivity	4.5 µV/e ⁻
Typical readout noise	3 e ⁻ at 20 kHz
Typical pixel charge capacity	100 ke ⁻ /pixel
Typical dark signal (20°C)	250 e ⁻ /pixel/second

OVERVIEW

Back illumination technology in combination with high dynamic range make this device well suited to demanding spectroscopy applications.

This device operates in advanced inverted mode (AIMO) for low dark current.

The readout register has 4x the charge capacity of an active pixel to support charge binning and includes a gate-controlled dump drain for fast dumping of unwanted data.

The output amplifier can operate in both a low noise and high signal modes with zero light emission.

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Template: 1B300000-DPF Ver 1

A1A-100024 Version 12, Aug 2025

CM5005133

PERFORMANCE

		Min	Typical	Max	Units	Note
Peak charge storage (image)		-	100,000	-	e ⁻ /pixel	1, 2(a)
Peak charge storage (register/SW)		-	400,000	-	e ⁻ /pixel	1, 2(b)
Peak output voltage		-	450	-	mV	
Output node capacity	Low noise mode	-	150,000	-	e ⁻	1, 2(c)
	High signal mode	-	600,000	-	e ⁻	
Output amplifier responsivity	Low noise mode	3.0	4.5	6.0	μV/e ⁻	
	High signal mode	-	1.5	-	μV/e ⁻	1
Readout noise	Low noise mode	-	3	4	e ⁻ rms	3
	High signal mode	-	6	-		1
Readout frequency		-	20	3000	kHz	4
Dark signal responsivity	293 K	-	250	500	e ⁻ /pixel/s	5
Dark signal non-uniformity (std. deviation)	293 K	-	60	-	e ⁻ /pixel/s	6
Binned column dark signal non-uniformity	293 K	-	7	15	e ⁻ /pixel/s	
Charge transfer efficiency	Parallel	99.9990	99.9999	-	%	1, 7
	Serial	99.9990	99.9993	-	%	

NOTES

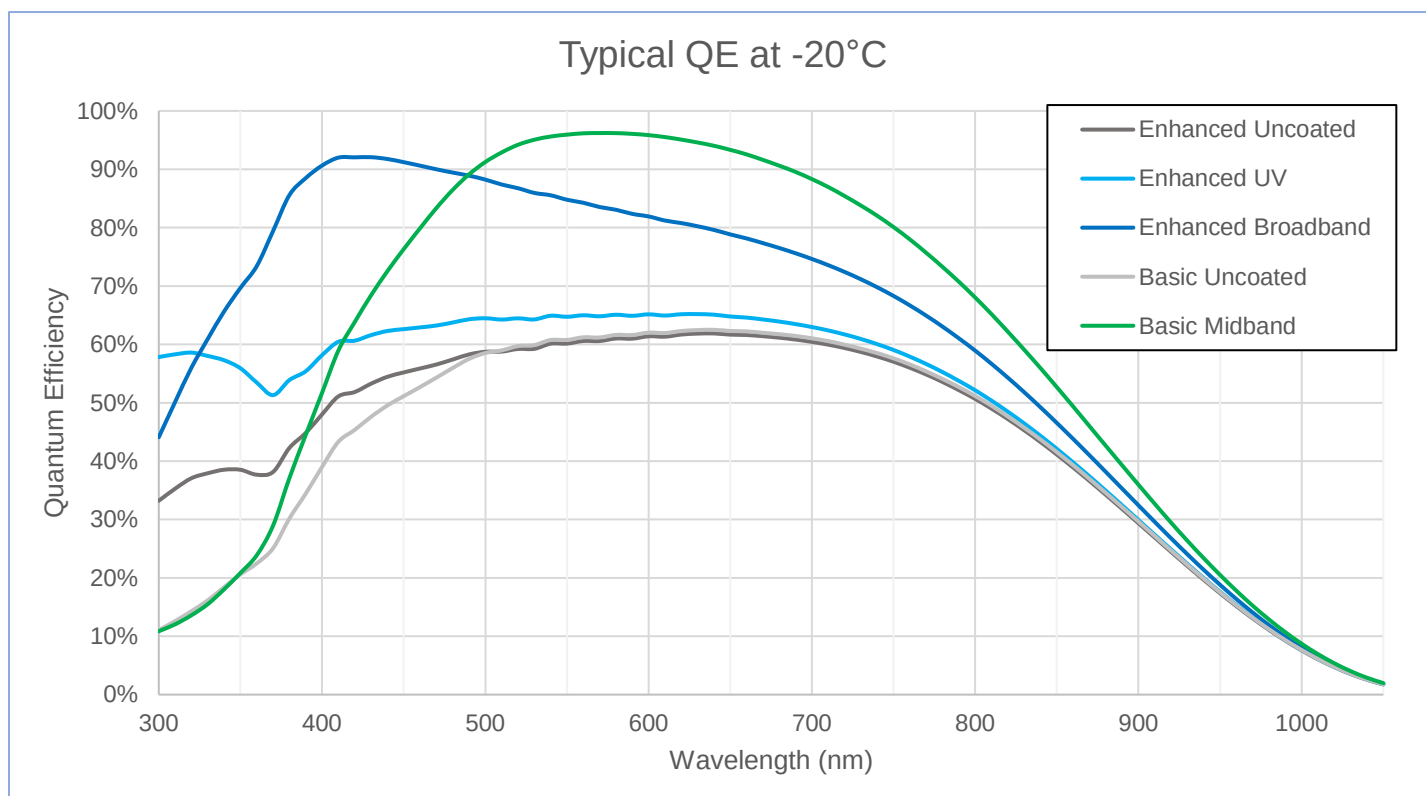
- Not measured as production test.
- (a) Signal level at which resolution begins to degrade.
(b) The summing well capacity limited the charge in the register.
(c) The signal handled by the output node (for linear operation) varies with mode as shown. Values are inferred by design and not factory tested.
- Measured at OS with correlated double sampling at 20 kHz pixel rate in low noise mode.
- Readout above 3000 kHz can be achieved but performance to the parameters given cannot be guaranteed.
- Dark signal is typically measured at a device temperature of 173 K. It is a strong function of temperature and the typical average (background) dark signal at any temperature T (Kelvin) between 150 K and 300 K is given by:

$$Q_d/Q_{do} = 1.14 \times 10^6 T^3 e^{-9080/T}$$
 where Q_{do} is the dark current at 293 K. Note that this is typical performance and some variation may be seen between devices. Below 230 K additional dark current components with a weaker temperature dependence may become significant.
- Dark signal non-uniformity (DSNU) is defined as the 1σ variation of the dark signal.
- Measured with a ⁵⁵Fe X-ray source. The CTE value is quoted for the complete clock cycle (i.e. not per phase).

SPECTRAL RESPONSE

The table below gives guaranteed minimum values of the spectral response at -20°C.

Wavelength (nm)	Minimum Response (QE)					Max PRNU (1 σ)	
	Basic Process		Enhanced Process				
	Uncoated	Midband Coated	Uncoated	UV Coated	Broadband Coated		
300	-	-	-	45	-		
350	10	15	20	45	50	5	%
400	25	40	35	55	80	3	%
500	55	85	50	60	80	3	%
650	50	85	50	60	72	3	%
900	25	25	25	25	25	5	%



NOTES

8. Devices with alternative or custom spectral response may be available by special request. Consult Teledyne e2v.

COSMETIC SPECIFICATIONS

Maximum allowed defect levels are indicated below.

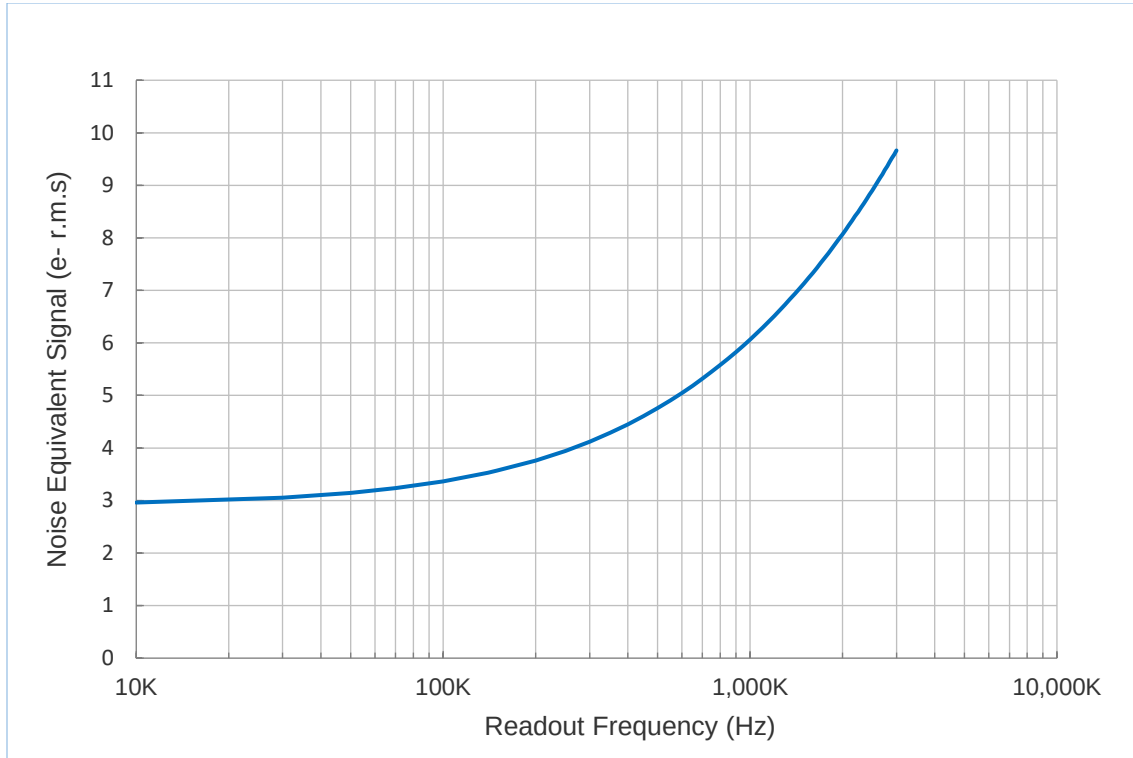
Grade		0	1
Column defects	Black	0	1
	White	0	0
Spots	Black	40	80
	White	20	30
Traps > 200e-		1	2
Spikes	Level 1	15	20
	Level 2	3	4

Cosmetic definitions

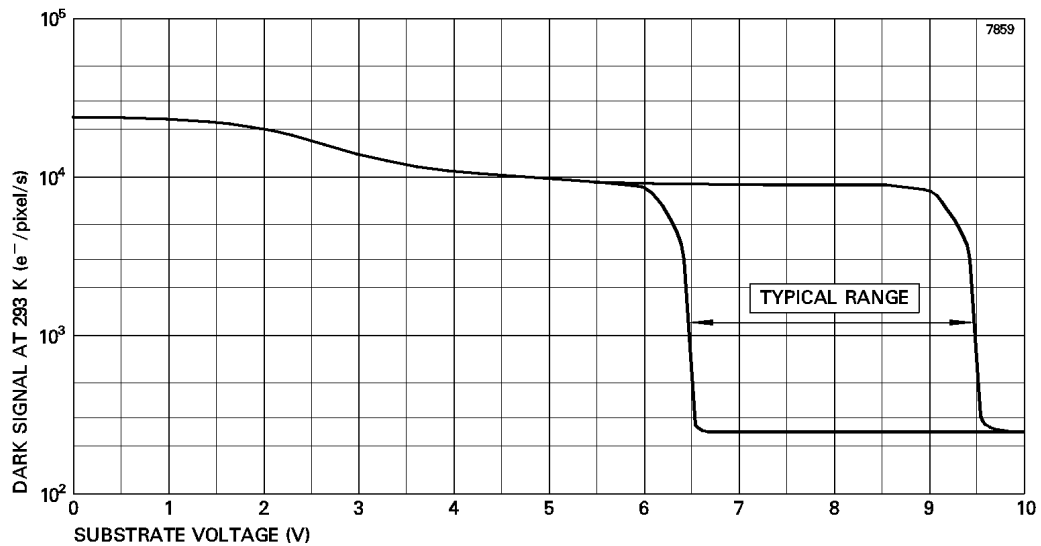
Black spots	A black spot defect is a pixel with a photo-response less than 80% of the local mean.
White spots	Are counted when they have a generation rate 100 times the specified maximum dark signal generation rate at 293 K (measured between 233 and 273 K). The amplitude of white spot blemishes decreases rapidly with temperature and is given by: $Q_d/Q_{d0} = 122T^3e^{6400/T}$
Column defects	A column is counted as a defect if it contains at least 9 white or dark single pixel defects.
Traps	A trap causes charge to be temporarily held in a pixel and these are counted as defects if the quantity of trapped charge is greater than 200 e-.
Spikes	Are measured with the image fully binned into the register. Level 1 spikes are those above 50 ke-/column. Level 2 spikes are those above 200 ke-/column.

AMPLIFIER READ NOISE

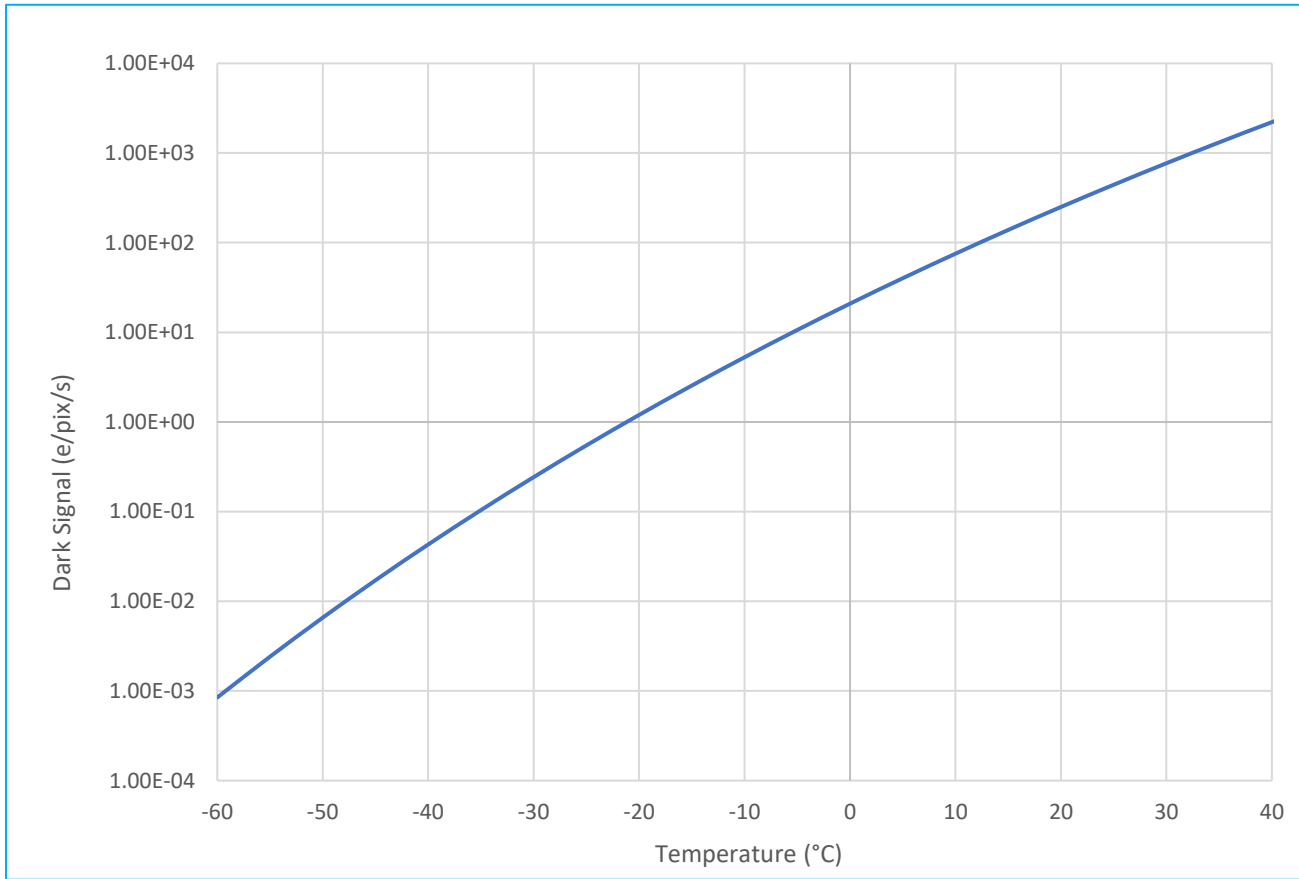
The theoretical variation of read noise with operating frequency is shown below. (If measured using clamp and sample).



TYPICAL VARIATION OF DARK SIGNAL WITH SUBSTRATE VOLTAGE



TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE



DEFINITIONS

Back-thinning

A back-thinned CCD is fabricated on the front surface of the silicon and is subsequently processed for illumination from the reverse side. This avoids loss of transmission in the electrode layer (particularly significant at shorter wavelengths or with low energy X-rays). This process requires the silicon to be reduced to a thin layer by a combination of chemical and mechanical means. The surface is “passivated” and an anti-reflection coating may be added.

AR Coating

Anti-reflection coatings are normally applied to the back illuminated CCD to further improve the quantum efficiency. Standard coatings optimise the response in the visible, ultra-violet or infrared regions. For X-ray detection an uncoated device may be preferable.

Inverted Mode

An inverted mode CCD has an additional implant that allows charge integration to be carried out with all clock phases low. With a high voltage applied to the substrate (typically +9 V) this causes the whole of the device to be flooded with holes (inverted or pinned), which suppresses the surface component of dark signal. This leaves only the much lower bulk component, reducing the overall dark signal by a factor of approximately 100.

Inverted mode operation is also referred to as multi-phase pinning (MPP).

Readout Noise

Readout noise is the random noise from the CCD output stage in the absence of signal. This noise introduces a random fluctuation in the output voltage that is superimposed on the detected signal.

The method of measurement involves reverse-clocking the register and determining the standard deviation of the output fluctuations, and then converting the result to an equivalent number of electrons using the known amplifier responsivity.

Dark Signal

This is the output signal of the device with zero illumination. This typically consists of thermally generated electrons within the semiconductor material, which are accumulated during signal integration. Dark signal is a strong function of temperature as described in note 3.

Correlated Double Sampling

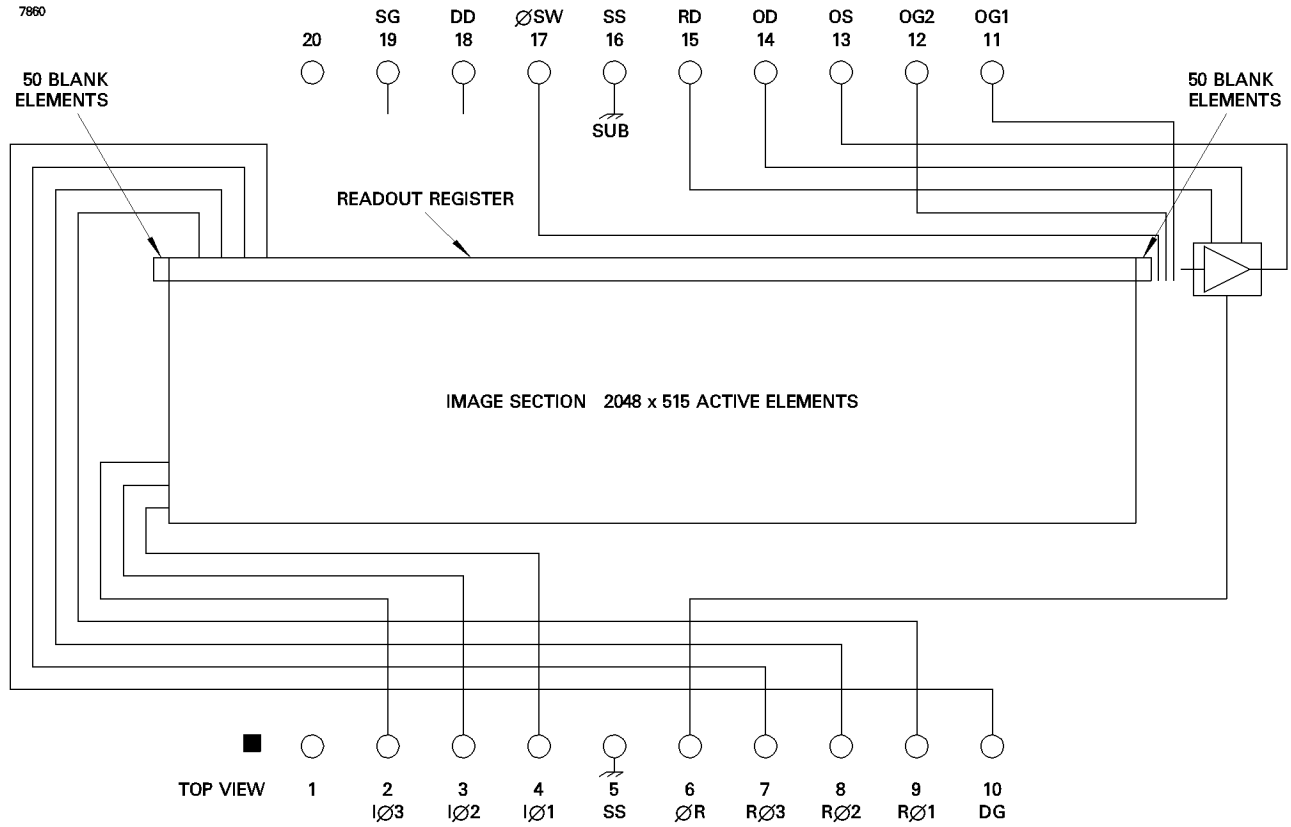
A technique for reducing the noise associated with the charge detection process by subtracting a first output sample taken just after reset from a second sample taken with charge present.

Charge Transfer Efficiency

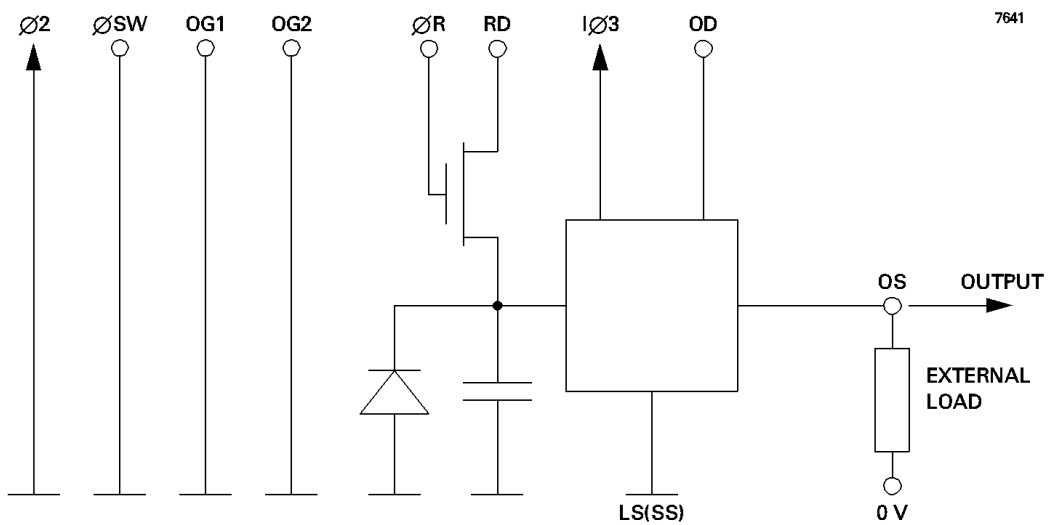
The fraction of charge stored in a CCD element that is transferred to the adjacent element by a single clock cycle. The charge not transferred remains in the original element, possibly in trapping states and may possibly be released into later elements. The value of CTE is not constant but varies with signal size, temperature, and clock frequency.

ARCHITECTURE

Chip Schematic



OUTPUT CIRCUIT



ELECTRICAL INTERFACE

CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

Note that the hyphenated suffix symbols (e.g. ØR-H) indicate to which output any register or amplifier pin relates.

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 12)			MAX RATINGS with respect to V _{SS} (V)
			Min	Typical	Max	
1	-	No connection	-			-
2	IØ3	Image section, phase 3 (clock pulse)	8	12	15	±20 V
3	IØ2	Image section, phase 2 (clock pulse)	8			±20 V
4	IØ1	Image section, phase 1 (clock pulse)	12	15		±20 V
5	SS	Substrate	8	12	15	-
6	ØR	Output reset pulse	8	9.5	11	±20 V
7	RØ3	Readout register, phase 3 (clock pulse)	8	12	15	±20 V
8	RØ2	Readout register, phase 2 (clock pulse)	8	12	15	±20 V
9	RØ1	Readout register, phase 1 (clock pulse)	8	12	15	±20 V
10	DG	Dump gate (see note 13)	8	12	15	±20 V
11	OG1	Output gate 1	-	0	-	±20 V
12	OG2	Output gate 2 (see note 14)	2	3	4	±20 V
13	OS	Output transistor source	see note 15			-
14	OD	Output drain	8	9	10.5	-0.3 to +25 V
15	RD	Reset transistor drain	9	11	12	-0.3 to +25 V
16	SS	Substrate	9	11	12	-0.3 to +25 V
17	ØSW	Summing well (see note 16)	8	9	10.5	-
18	DD	Diode drain	9	11	12	±20 V
19	SG	Spare gates	0	0	V _{SS} + 19	-0.3 to +25 V
20	-	No connection	-			-

NOTES

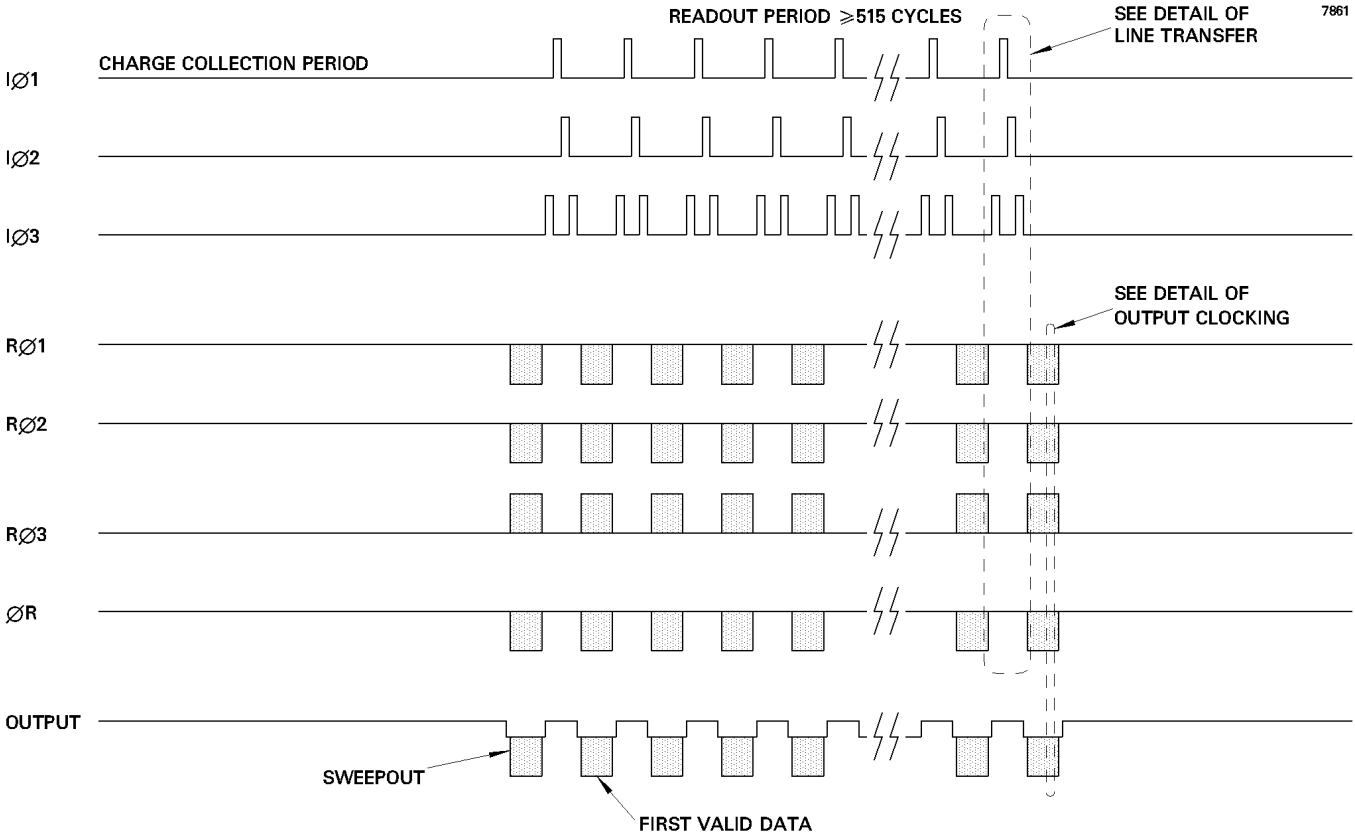
9. If all voltages are set to the typical values, operation at or close to specification should be obtained. Some adjustment within the range specified may be required to optimise performance.
10. Maximum voltages between pairs of pins: OS to OD ± 15 V
11. Maximum current through any source or drain pin: 10 mA
12. Readout register clock pulse low levels + 1 V; other clock low levels 0 ± 0.5 V.
13. Non-charge dumping level shown. For charge dumping, DG should be pulsed to 12 ± 2 V.
14. Use OG2 = OG1 + 1 V for normal, low noise mode, or 20 V for low responsivity, high signal mode.
15. Not critical; can be a 1 -- 5 mA constant current source, or 5 -- 10 kΩ resistor.
16. For normal operation, the summing well should be clocked as RØ3.
17. The amplifier has a DC restoration circuit, which is activated internally whenever IØ3 is pulsed high

ELECTRICAL INTERFACE CHARACTERISTICS

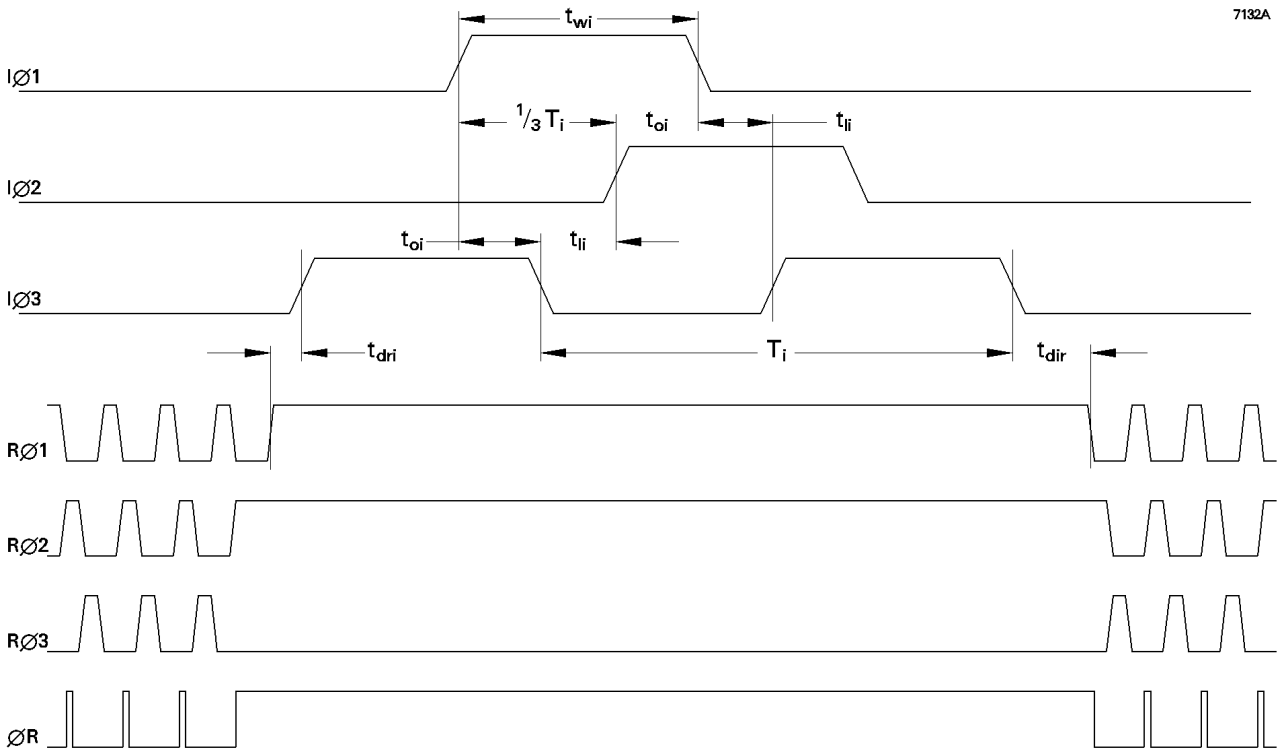
Electrode capacitances (defined at mid-clock level)

	Typical	Units
IØ/IØ inter-phase	5	nF
RØ/RØ inter-phase	80	nF
IØ/SS	15	nF
RØ/SS	150	pF
Output impedance	350	Ω

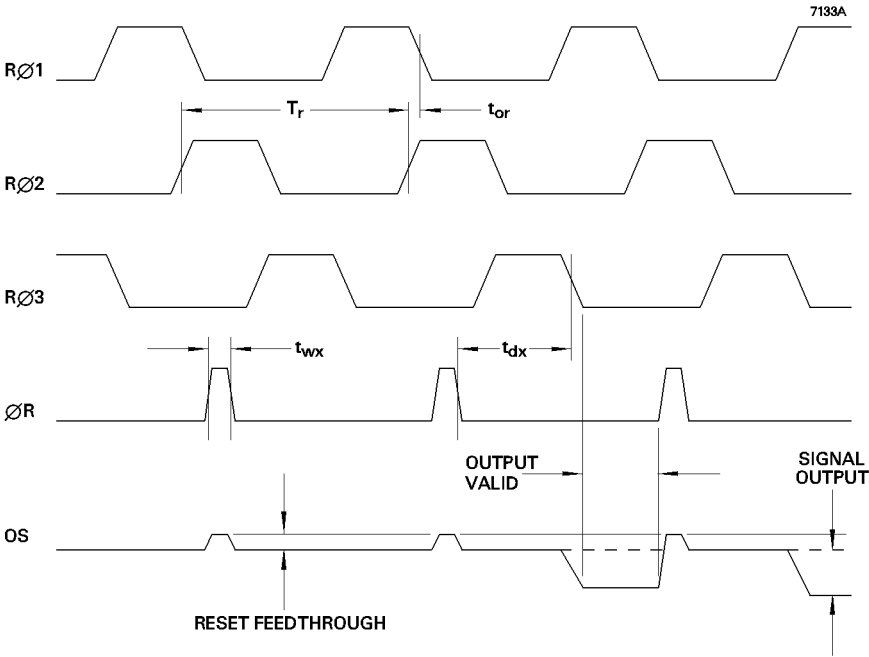
FRAME READOUT TIMING DIAGRAM



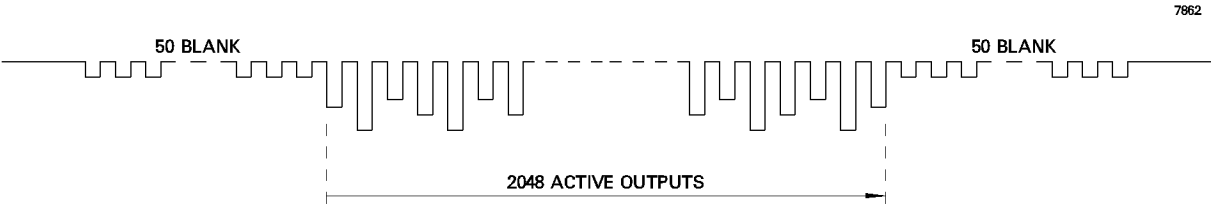
DETAIL OF LINE TRANSFER



DETAIL OF OUTPUT CLOCKING (Operation through both outputs)



LINE OUTPUT FORMAT



CLOCK TIMING REQUIREMENTS

Symbol	Description	Minimum	Typical	Maximum	Units
T_i	Image clock period	15	30	see note 18	μs
t_{wi}	Image clock pulse width	7	15	see note 18	μs
t_{ri}	Image clock pulse rise time (10 to 90%)	0.5	2	$0.5t_{oi}$	μs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	2	$0.5t_{oi}$	μs
t_{oi}	Image clock pulse overlap	3	5	$0.2T_i$	μs
t_{li}	Image clock pulse, two phase low	3	5	$0.2T_i$	
t_{dir}	Delay time, $I\emptyset$ stop to $R\emptyset$ start	3	5	see note 18	μs
t_{dri}	Delay time, $R\emptyset$ stop to $I\emptyset$ start	1	2	see note 18	μs
T_r	Output register clock cycle period	333	see note 19	see note 18	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.2T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	20	$0.5t_{rr}$	$0.2T_r$	ns
t_{dx}	Delay time, $\emptyset R$ low to $R\emptyset 3$ low	30	$0.5T_r$	$0.8T_r$	ns

NOTES

18. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.

19. As set by the readout period.

HEALTH AND SAFETY HAZARDS

Teledyne e2v devices are safe to handle and operate, provided that the relevant precautions stated herein are observed. Teledyne e2v does not accept responsibility for damage or injury resulting from the use of devices it produces. Equipment manufacturers and users must ensure that adequate precautions are taken. Appropriate warning labels and notices must be provided on equipment incorporating Teledyne e2v devices and in operating manuals.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (pins 2, 3, 4, 6, 7, 8, 9, 12, 19) but not to the other pins.

The devices are assembled in a clean room environment. Teledyne e2v recommend that similar precautions are taken to avoid contaminating the active surface.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to an ionising radiation. Users planning to use CCDs in a high radiation environment are advised to contact Teledyne e2v.

TEMPERATURE LIMITS

	Min	Typical	Max
Storage	153	-	373 K
Operating.....	153	233	323 K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling..... 5 K/min

PART REFERENCES

Variant	Illumination	Enhanced BSI Process	Silicon	AR Coating	Fringe Suppression
CCD42-10-G-113	BSI	Yes	Standard	Uncoated	No
CCD42-10-G-313	BSI	Yes	Standard	UV	No
CCD42-10-G-319	BSI	Yes	Standard	Broadband	No
CCD42-10-G-351	BSI	No	Standard	Uncoated	No
CCD42-10-G-970	BSI	No	Standard	Midband	No

Grade Definitions

Grade 0	Super Grade	Meets all Grade 0 performance parameters and cosmetic parameters
Grade 1	Science Grade	Meets all Grade 1 performance parameters and cosmetic parameters
Grade 5	Engineering Grade	Electrically functional with no performance or cosmetic parameter guarantees
Grade 6	Mechanical Grade	Non-functional. Mechanically representative only.

NOTES

21. G = Grade (e.g. 1)

22. Additional variants may be available to custom order. Consult Teledyne e2v for more information.