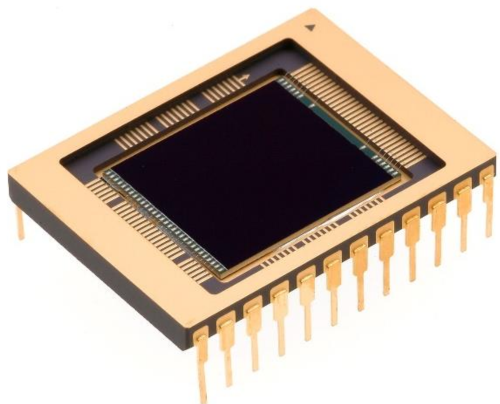
CCD47-10

1MP BSI CCD Sensor



KEY FEATURES

- 1024 x 1024 nominal active pixels (1056 x 1027 usable)
- 13µm square pixels
- Back Illuminated
- Full-frame operation
- Very low noise output amplifiers
- Gated dump drain on output
- Enhanced BSI options for UV/Blue
- Deep depletion options for Red/NIR
- Uncoated options for soft X-Ray

TYPICAL APPLICATIONS

- Scientific Imaging
- X-Ray Imaging
- Spectroscopy

PART REFERENCES

Please see last page for full list of available parts.

Also available front illuminated.

GENERAL DATA

Format		
Image Area		13.3 × 13.3 mm
Active Pixels		1056(H) x 1027(V)
Pixel Size		13 × 13 µm
Number of output amplifiers		2
Package		
Package Size		22.6 x 29.9 mm
Number of Pins		24
Inter-pin Spacing		2.54 mm
Window Material		Removable Glass
Package Type		Ceramic DIL array
Performance		
Maximum readout frequency		5 MHz
Output amplifier sensitivity		4.5 µV/e^-
Typical readout noise		2 e^- at 20 kHz
Typical pixel charge capacity	AIMO	100 ke^-/pixel
	NIMO	120 ke^-/pixel
Typical dark signal (20°C)	AIMO	250 e^-/pixel/s
	NIMO	20,000 e^-/pixel/s

OVERVIEW

Back illumination technology in combination with high dynamic range make this device well suited to demanding scientific applications. Wide range of variants available.

This device is available in either advanced inverted mode (AIMO) for low dark current or non-inverted mode (NIMO) for higher charge capacity and wider range of options.

The device has a single serial register with outputs at both ends. Charge can be transferred to either output or split between both. A gated dump drain is included to allow the fast dumping of unwanted charge.

Teledyne UK Limited, Waterhouse Lane, Chelmsford, Essex CM1 2QU United Kingdom Teledyne UK Ltd. is a Teledyne Technologies company.
Telephone: +44 (0)1245 493493 Facsimile: +44 (0)1245 492492
Contact Teledyne e2v online at www.teledynespaceimaging.com/en-us/contact-us

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5005507
Approved for public release: Teledyne e2v APPROVED (5005507)

PERFORMANCE

NIMO

		Min	Typical	Max	Units	Note
Peak charge storage (image)		-	120,000	-	e^-/pixel	1, 2(a)
Output node capacity		-	600,000	-	e^-/pixel	1, 2(b)
Peak output voltage (unbinned)		-	540	-	mV	
Output amplifier responsivity	Low noise mode	3.0	4.5	6.0	$\mu V/e^-$	
Readout noise	Low noise mode	-	2	4	e^- rms	3
Readout frequency		-	20	5,000	kHz	4
Dark signal responsivity	Standard Silicon	-	20,000	40,000	e^-/pixel/s	5, 6
	Deep Depleted	-	43,000	85,000		
Dark signal non-uniformity (std. deviation)	Standard Silicon	-	1,000	2,000	e^-/pixel/s	5, 7
	Deep Depleted	-	4,300	8,500		
Charge transfer efficiency	Parallel	-	99.9999	-	%	1, 8
	Serial	-	99.9993	-	%	
Response non-linearity (std. deviation)		-	3	10	%	

AIMO

		Min	Typical	Max	Units	Note
Peak charge storage (image)		-	100,000	-	e^-/pixel	1, 2(a)
Output node capacity		-	600,000	-	e^-/pixel	1, 2(b)
Peak output voltage (unbinned)		-	450	-	mV	
Output amplifier responsivity	Low noise mode	3.0	4.5	6.0		
Readout noise	Low noise mode	-	2	4	e^- rms	3
Readout frequency		-	20	5,000	kHz	4
Dark signal responsivity		-	250	500	e^-/pixel/s	5, 6
Dark signal non-uniformity (std. deviation)		-	60	125	e^-/pixel/s	5, 7
Charge transfer efficiency	Parallel	-	99.9999	-	%	1, 8
	Serial	-	99.9993	-	%	

See notes overleaf.

NOTES

1. Not measured as production test.
2. (a) Signal level at which resolution begins to degrade.

   (b) The signal handled by the output node (for linear operation) varies with mode as shown. Values are inferred by design and not factory tested.
3. Measured at a pixel readout frequency of 18 KHz for NIMO and 20 kHz for AIMO using a dual-slope integrator technique (i.e. correlated double sampling).
4. Readout above 5 MHz into a 15 pF load can be achieved but performance to the parameters given cannot be guaranteed.
5. Test carried out at 243 K for NIMO and 253 K for AIMO and scaled to 293 K using the formulas in note 6.
6. The typical average (background) dark signal at any temperature T (kelvin) between 233 K and 293 K and Vss + 9.5V may be estimated from:

   NIMO: $Qd/Qd0 = 122T^{3}e^{-6400/T}$

   AIMO: $Qd/Qdo = 1.14 \times 10^{6}T3e^{-9080/T}$

   where Qdo is the dark current at 293 K. Note that this is typical performance and some variation may be seen between devices. Below 230 K additional dark current components with a weaker temperature dependence may become significant.
7. Excluding white defects.
8. CCD characterisation measurement using charge generated by X-ray photons of known energy.

SPECTRAL RESPONSE

NIMO

The table below gives guaranteed minimum values of the spectral response at -30°C.

Wavelength (nm)	Minimum Response (QE)				Max PRNU (1 σ)	
	Standard Silicon	Deep Depletion Silicon				
	Enhanced Process		Basic Process			
	UV Coated (see Note 9)	ML2 Coated	NIR Coated	Uncoated		
300	45	-	-	-	-	**%**
350	45	30	15	10	-	**%**
400	55	75	30	25	3	**%**
500	60	75	50	50	-	**%**
650	60	80	75	55	3	**%**
900	22	65	65	40	5	**%**

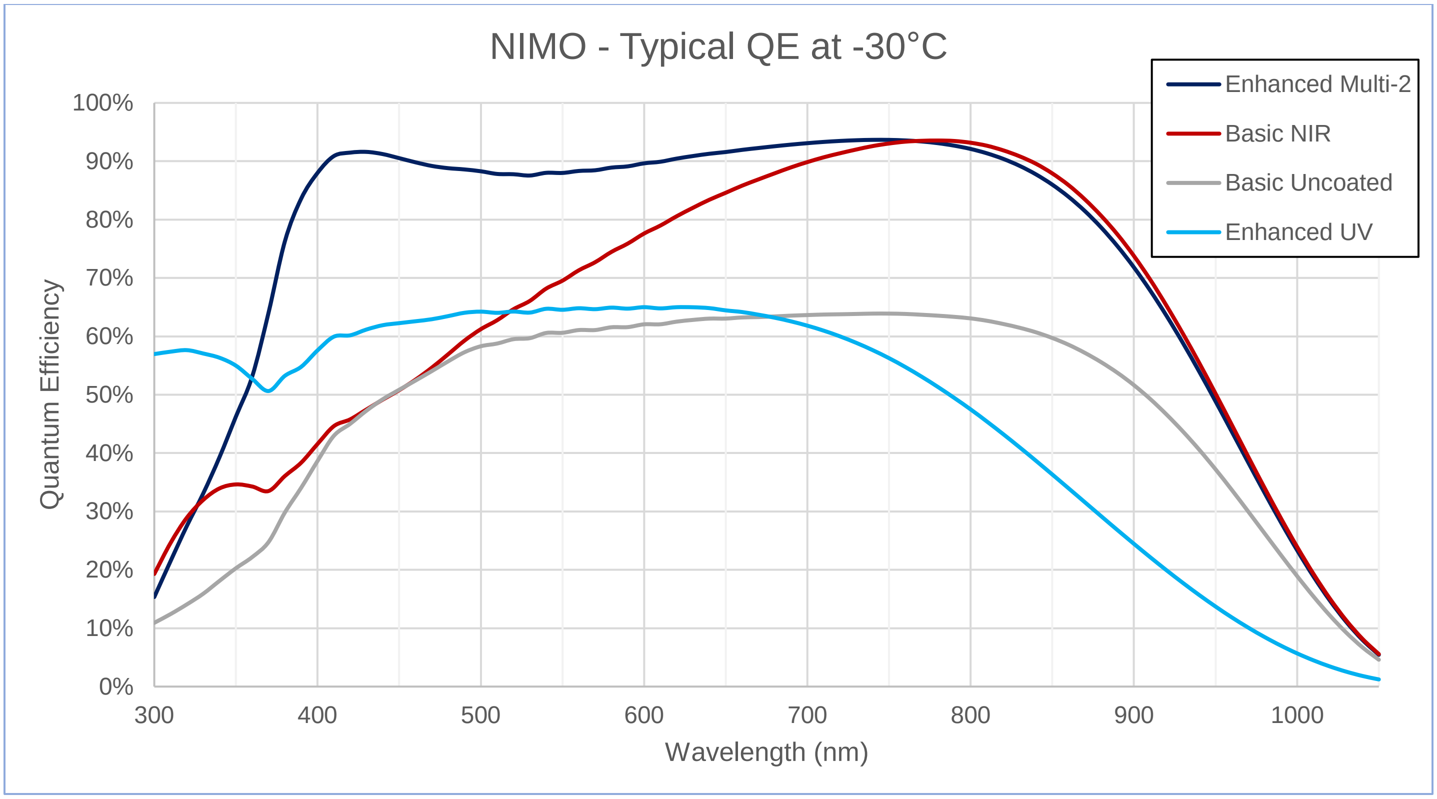
AIMO

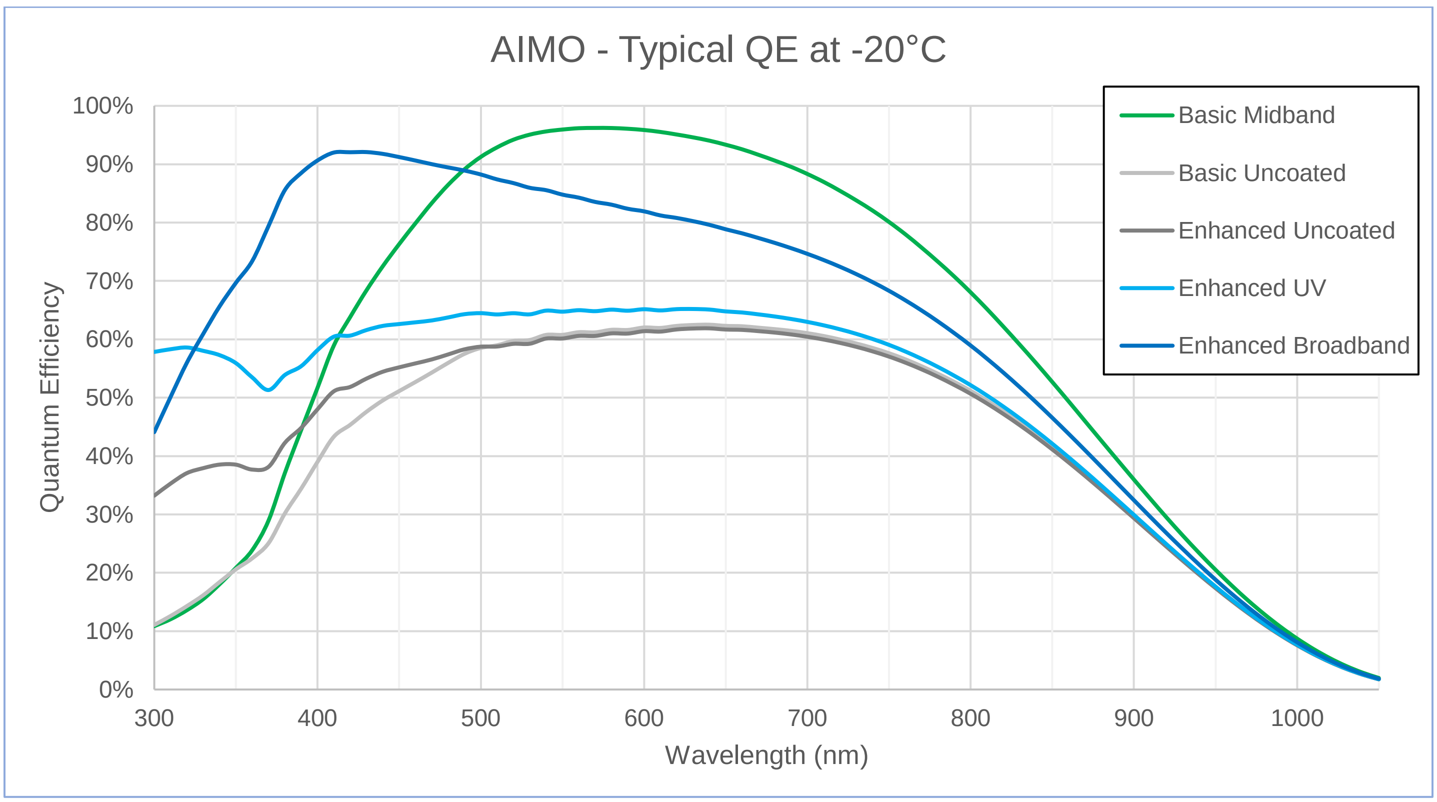
The table below gives guaranteed minimum values of the spectral response at -20°C.

Wavelength (nm)	Minimum Response (QE)					Max PRNU (1 σ)	
	Enhanced Process			Basic Process			
	Uncoated	UV Coated	Broadband Coated	Uncoated	Midband Coated		
300	-	45	-	-	-	-	**%**
350	20	45	25	10	15	5	**%**
400	35	55	55	25	40	3	**%**
500	50	60	75	55	85	3	**%**
650	50	60	75	50	85	3	**%**
900	25	25	25	25	25	5	**%**

NOTES

9. Variant includes shielded anti-blooming which slightly reduces 900nm QE.
10. Devices with alternative or custom spectral response may be available by special request. Consult Teledyne e2v.


NIMO - Typical QE at -30°C
Enhanced Multi-2
Basic NIR
Basic Uncoated
Enhanced UV
Quantum Efficiency
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%
300
400
500
600
700
800
900
1000
Wavelength (nm)


AIMO - Typical QE at -20°C
Basic Midband
Basic Uncoated
Enhanced Uncoated
Enhanced UV
Enhanced Broadband
Quantum Efficiency
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%
300
400
500
600
700
800
900
1000
Wavelength (nm)

COSMETIC SPECIFICATIONS

Maximum allowed defect levels are indicated below.

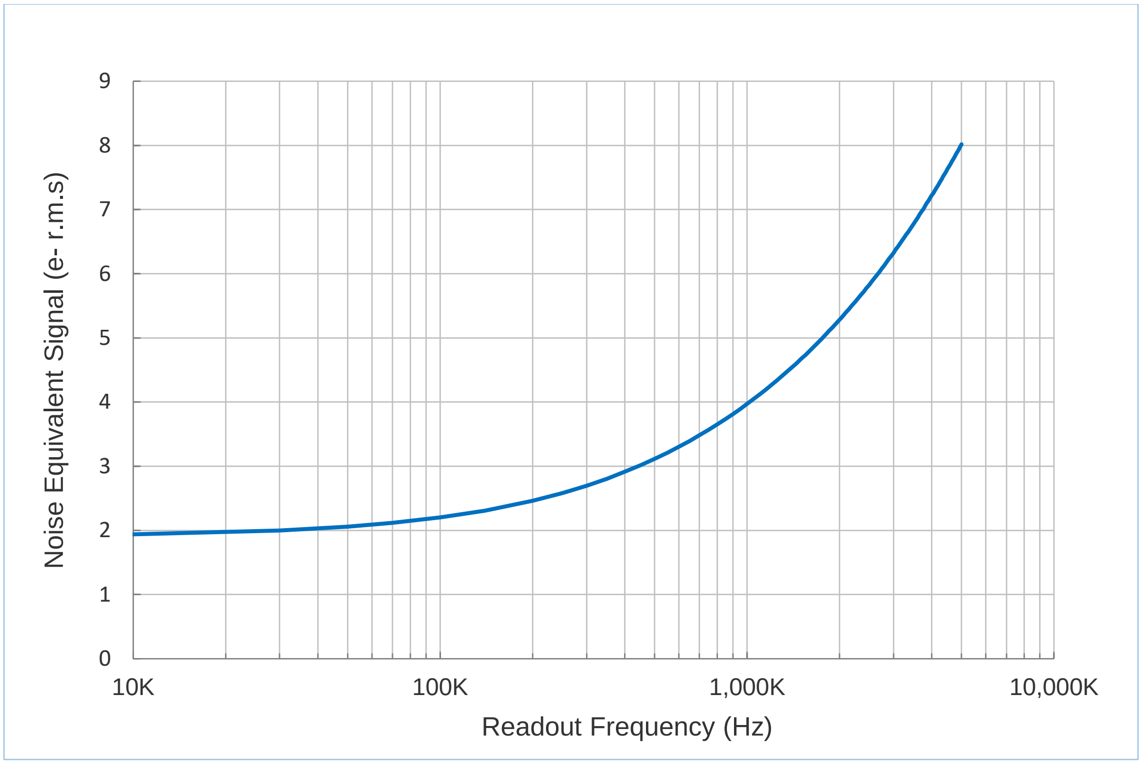
Grade		0	1
Column defects	**Black or Slipped**	0	2
	White	0	0
Spots	**Black**	50	100
	White	50	80
Traps > 200e-		2	5

Cosmetic definitions

Black spots	A black spot defect is a pixel with a photo-response less than 80% of the local mean at a signal level of approximately half full-well.
White spots (AIMO)	Are counted when they have a generation rate 125 times the specified maximum dark signal generation rate at 293 K (measured between 253 and 273 K). The amplitude of white spot blemishes decreases rapidly with temperature and is given by: $Q_d/Q_{d0} = 122T^3e^{6400/T}$
White spots (NIMO)	Are counted when they have a generation rate 20 times the specified maximum dark signal generation rate at 293 K (measured between 243 and 273 K). The amplitude of white spot blemishes decreases rapidly with temperature and is given by: $Q_d/Q_{d0} = 122T^3e^{6400/T}$
Column defects	A black or white column is counted as a defect if it contains at least 21 white or dark single pixel defects. A slipped column is counted if it has an amplitude greater than 200 e-. Minimum separation between adjacent black columns is 50 pixels.
Traps	A trap causes charge to be temporarily held in a pixel and these are counted as defects if the quantity of trapped charge is greater than 200 e-.

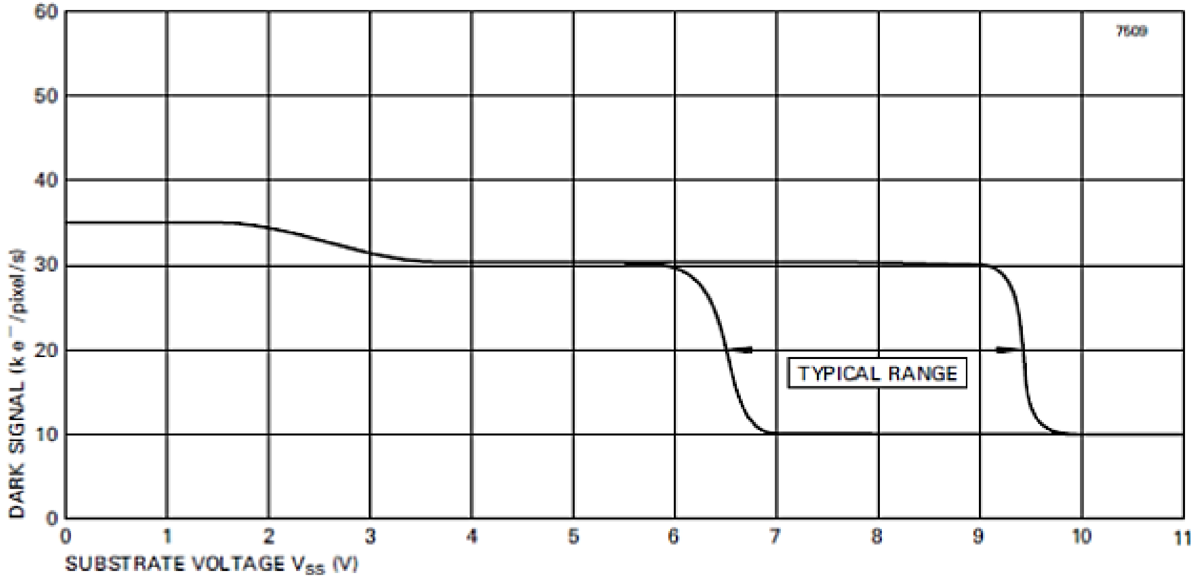
AMPLIFIER READ NOISE

The theoretical variation of read noise with operating frequency is shown below. (If measured using clamp and sample).

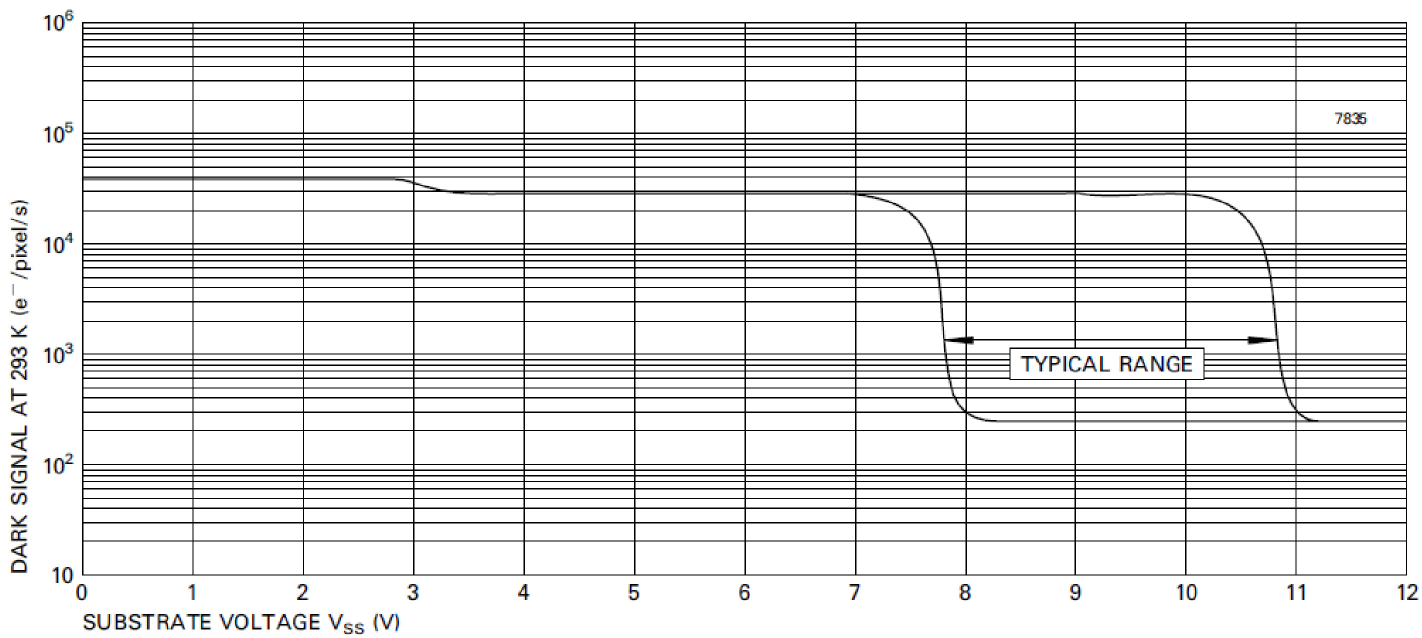


TYPICAL VARIATION OF DARK SIGNAL WITH SUBSTRATE VOLTAGE

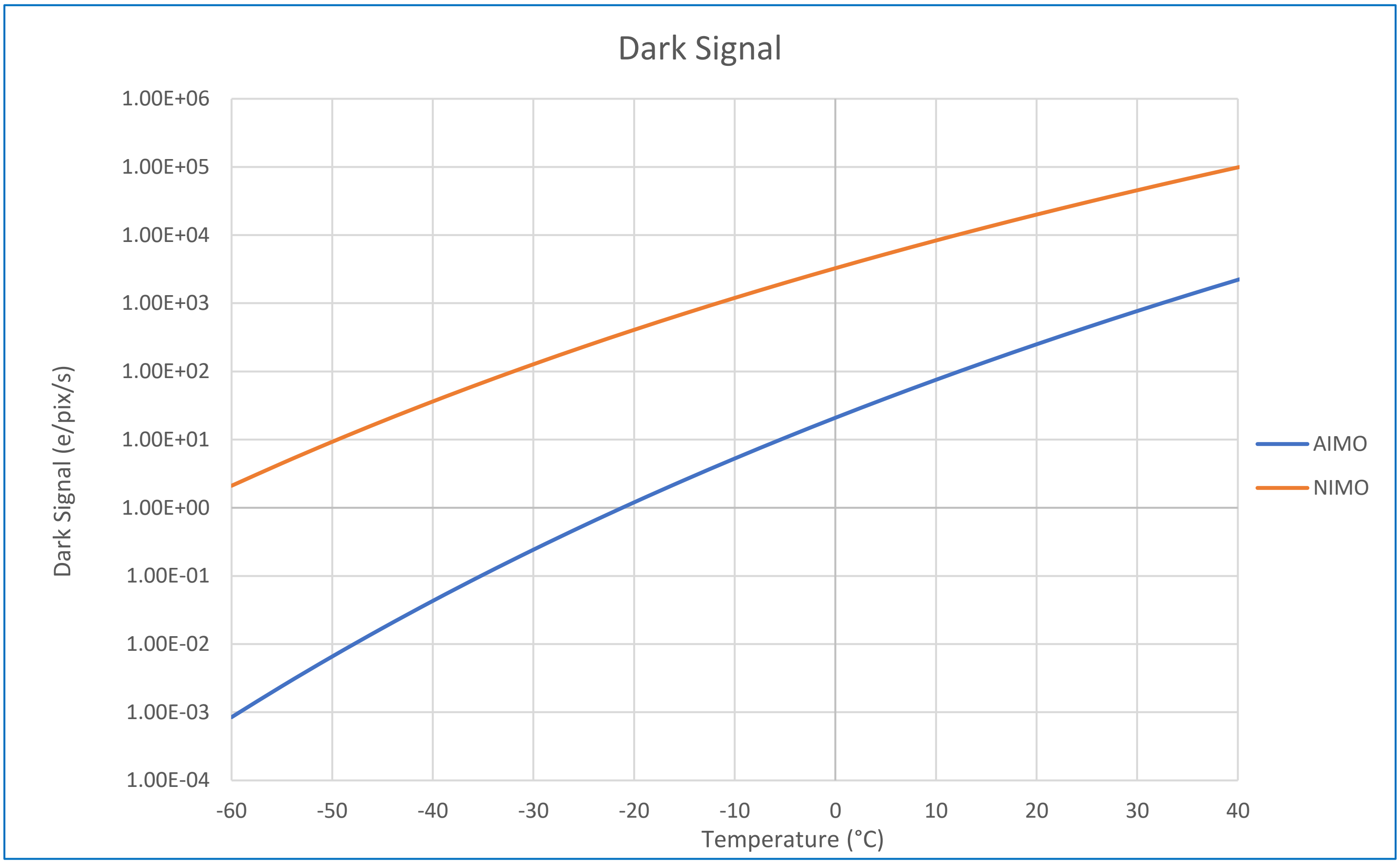
NIMO



AIMO



TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE



DEFINITIONS

Back-thinning

A back-thinned CCD is fabricated on the front surface of the silicon and is subsequently processed for illumination from the reverse side. This avoids loss of transmission in the electrode layer (particularly significant at shorter wavelengths or with low energy X-rays). This process requires the silicon to be reduced to a thin layer by a combination of chemical and mechanical means. The surface is “passivated” and an anti-reflection coating may be added.

AR Coating

Anti-reflection coatings are normally applied to the back illuminated CCD to further improve the quantum efficiency. Standard coatings optimise the response in the visible, ultra-violet or infrared regions. For X-ray detection an uncoated device may be preferable.

Inverted Mode

An inverted mode CCD has an additional implant that allows charge integration to be carried out with all clock phases low. With a high voltage applied to the substrate (typically +9 V) this causes the whole of the device to be flooded with holes (inverted or pinned), which suppresses the surface component of dark signal. This leaves only the much lower bulk component, reducing the overall dark signal by a factor of approximately 100.

Inverted mode operation is also referred to as multi-phase pinning (MPP).

Readout Noise

Readout noise is the random noise from the CCD output stage in the absence of signal. This noise introduces a random fluctuation in the output voltage that is superimposed on the detected signal.

The method of measurement involves reverse-clocking the register and determining the standard deviation of the output fluctuations, and then converting the result to an equivalent number of electrons using the known amplifier responsivity.

Dark Signal

This is the output signal of the device with zero illumination. This typically consists of thermally generated electrons within the semiconductor material, which are accumulated during signal integration. Dark signal is a strong function of temperature as described in note 0.

Correlated Double Sampling

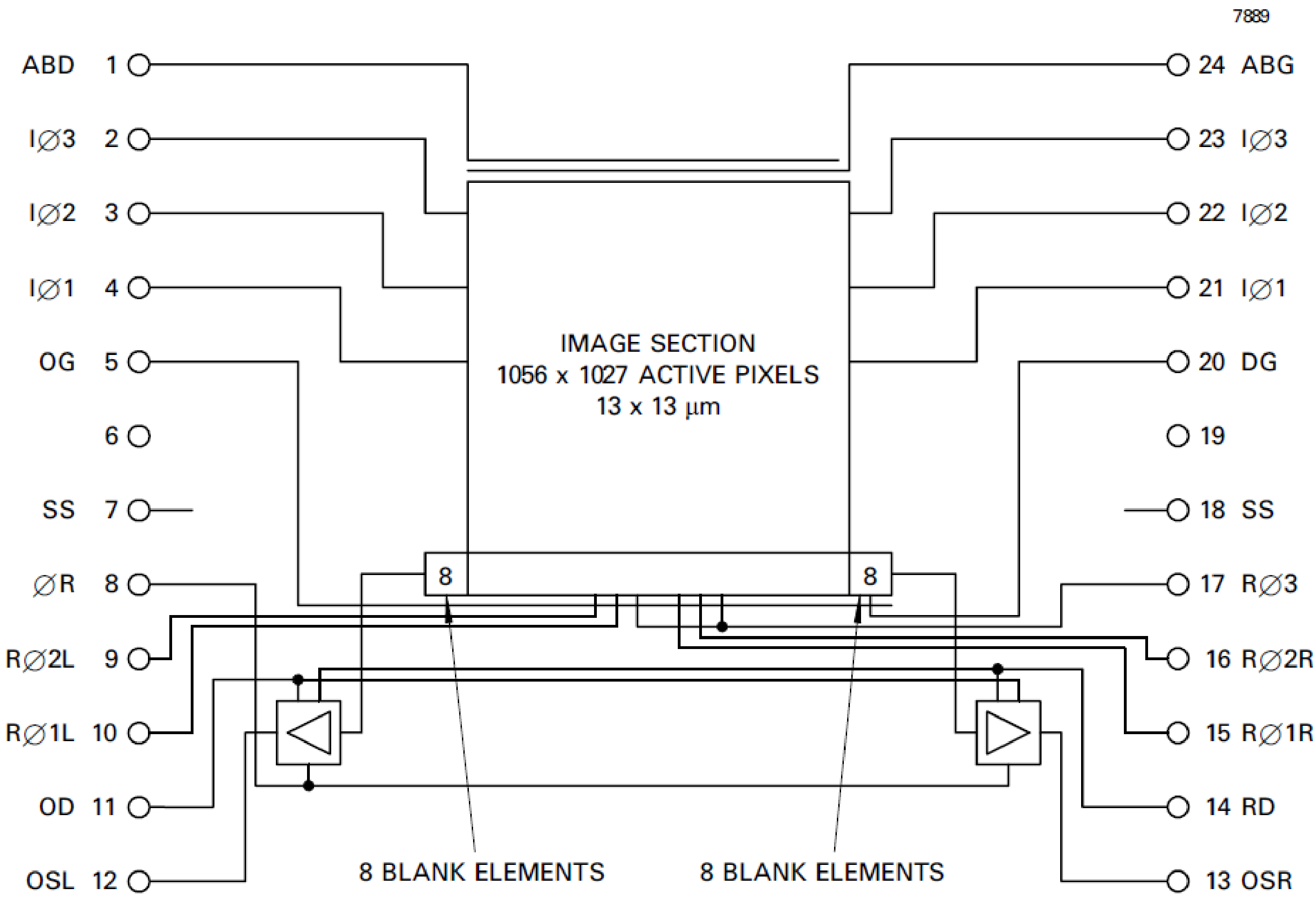
A technique for reducing the noise associated with the charge detection process by subtracting a first output sample taken just after reset from a second sample taken with charge present.

Charge Transfer Efficiency

The fraction of charge stored in a CCD element that is transferred to the adjacent element by a single clock cycle. The charge not transferred remains in the original element, possibly in trapping states and may possibly be released into later elements. The value of CTE is not constant but varies with signal size, temperature, and clock frequency.

ARCHITECTURE

Chip Schematic

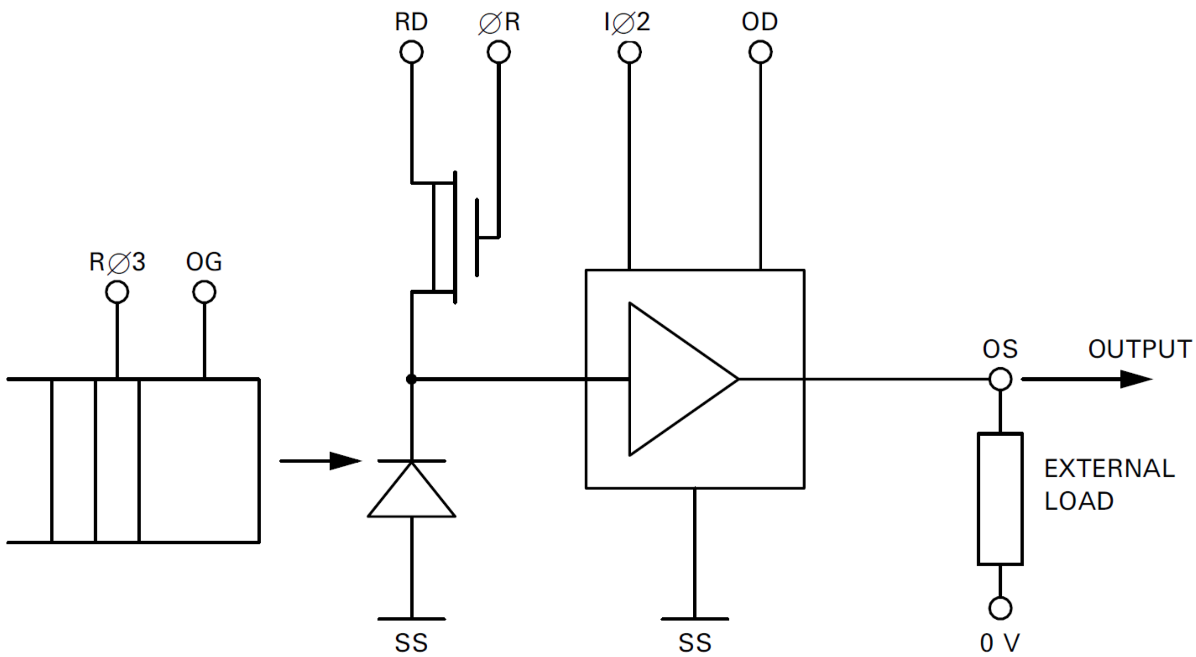


NOTES

11. Pins 6 and 19 are not connected.

OUTPUT CIRCUIT

7766A



NOTES

12. The amplifier has a DC restoration circuit which is internally activated whenever I∅2 is high.

13. Not critical; can be a 3 to 5mA constant current supply or an appropriate load resistor.

ELECTRICAL INTERFACE

CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

NIMO

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 15)			MAX RATINGS with respect to V_{SS} (V)
			Min	Typical	Max	
1	ABD	Anti-Blooming drain (see note 15)		V_{OD}		–0.3 to +25 V
2	I∅3	Image section, phase 3 (clock pulse)	8	12	15	±20 V
3	I∅2	Image section, phase 2 (clock pulse)	8	12	15	±20 V
4	I∅1	Image section, phase 1 (clock pulse)	8	12	15	±20 V
5	OG	Output Gate	1	2	5	±20 V
6	-	No connection		-		-
7	SS	Substrate	0	9	10	
8	∅R	Output reset pulse Left and Right amplifiers	8	12	15	±20 V
9	R∅2L	Readout register, phase 2 (clock pulse) Left section	8	10	15	±20 V
10	R∅1L	Readout register, phase 1 (clock pulse) Left section	8	10	15	±20 V
11	OD	Output transistor drain Left and right amplifiers	-	0	-	–0.3 to +25 V
12	OSL	Output transistor source Left amplifier		See note 16		–0.3 to +25 V
13	OSR	Output transistor source Right amplifier		See note 16		–0.3 to +25 V
14	RD	Reset transistor drain Left and right amplifier	15	17	19	–0.3 to +25 V
15	R∅1R	Readout register, phase 1 (clock pulse) Right section	8	10	15	±20 V
16	R∅2R	Readout register, phase 2 (clock pulse) Right section	8	10	15	±20 V
17	R∅3	Readout register, phase 3 (clock pulse) Left and right sections	8	10	15	±20 V
18	SS	Substrate	0	9	10	-
19	-	No connection		-		-
20	DG	Dump gate (see note 17)	-	0	-	±20 V
21	I∅1	Image section, phase 1 (clock pulse)	8	12	15	±20 V
22	I∅2	Image section, phase 2 (clock pulse)	8	12	15	±20 V
23	I∅3	Image section, phase 3 (clock pulse)	8	12	15	±20 V
24	ABG	Anti-Blooming gate	0	0	5	±20 V

Maximum voltages between pairs of pins:
pin 12 (OSL) to pin 11 (OD) .... ±15 V
pin 11 (OD) to pin 13 (OSR) .... ±15 V
Maximum output transistor current........... 10 mA

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 15)			MAX RATINGS with respect to V_{SS} (V)
			Min	Typical	Max	
1	ABD	Anti-Blooming drain (see note 15)		V_{OD}		–0.3 to +25 V
2	I∅3	Image section, phase 3 (clock pulse)	12	15	16	±20 V
3	I∅2	Image section, phase 2 (clock pulse)	12	15	16	±20 V
4	I∅1	Image section, phase 1 (clock pulse)	12	15	16	±20 V
5	OG	Output Gate	1	3	5	±20 V
6	-	No connection		-		-
7	SS	Substrate	8	9.5	11	
8	∅R	Output reset pulse Left and Right amplifiers	8	12	15	±20 V
9	R∅2L	Readout register, phase 2 (clock pulse) Left section	8	10	15	±20 V
10	R∅1L	Readout register, phase 1 (clock pulse) Left section	8	10	15	±20 V
11	OD	Output transistor drain Left and right amplifiers	27	29	32	–0.3 to +25 V
12	OSL	Output transistor source Left amplifier		See note 16		–0.3 to +25 V
13	OSR	Output transistor source Right amplifier		See note 16		–0.3 to +25 V
14	RD	Reset transistor drain Left and right amplifier	15	17	19	–0.3 to +25 V
15	R∅1R	Readout register, phase 1 (clock pulse) Right section	8	10	15	±20 V
16	R∅2R	Readout register, phase 2 (clock pulse) Right section	8	10	15	±20 V
17	R∅3	Readout register, phase 3 (clock pulse) Left and right sections	8	10	15	±20 V
18	SS	Substrate	8	9.5	11	-
19	-	No connection		-		-
20	DG	Dump gate (see note 17)	-	0	-	±20 V
21	I∅1	Image section, phase 1 (clock pulse)	12	15	16	±20 V
22	I∅2	Image section, phase 2 (clock pulse)	12	15	16	±20 V
23	I∅3	Image section, phase 3 (clock pulse)	12	15	16	±20 V
24	ABG	Anti-Blooming gate	0	0	5	±20 V

Maximum voltages between pairs of pins:
- pin 12 (OSL) to pin 11 (OD) .... ±15 V
- pin 11 (OD) to pin 13 (OSR) .... ±15 V

Maximum output transistor current........... 10 mA

NOTES

14. Readout register clock pulse low levels +1V; other clock low levels 0 ± 0.5V Maximum voltages between pairs of pins: OS to OD ± 15 V.
15. Drain not incorporated, but bias is still necessary.
16. 3 to 5V below OD. Connect to ground using a 3 to 5 mA current source or appropriate load resistor (typically 5 to 10kΩ).
17. Non-charge dumping level shown. For charge dumping, DG should be pulsed to 12 ± 2 V.
18. All devices will operate at the typical values given. However, some adjustment within the minimum to maximum range may be required to optimise performance for critical applications. It should be noted that conditions for optimum performance may differ from device to device.
19. With the RØ connections shown, the device will operate through the right-hand output only. In order to operate from both outputs RØ1 (L) and RØ2 (L) should be reversed.

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (defined at mid-clock level)

NIMO

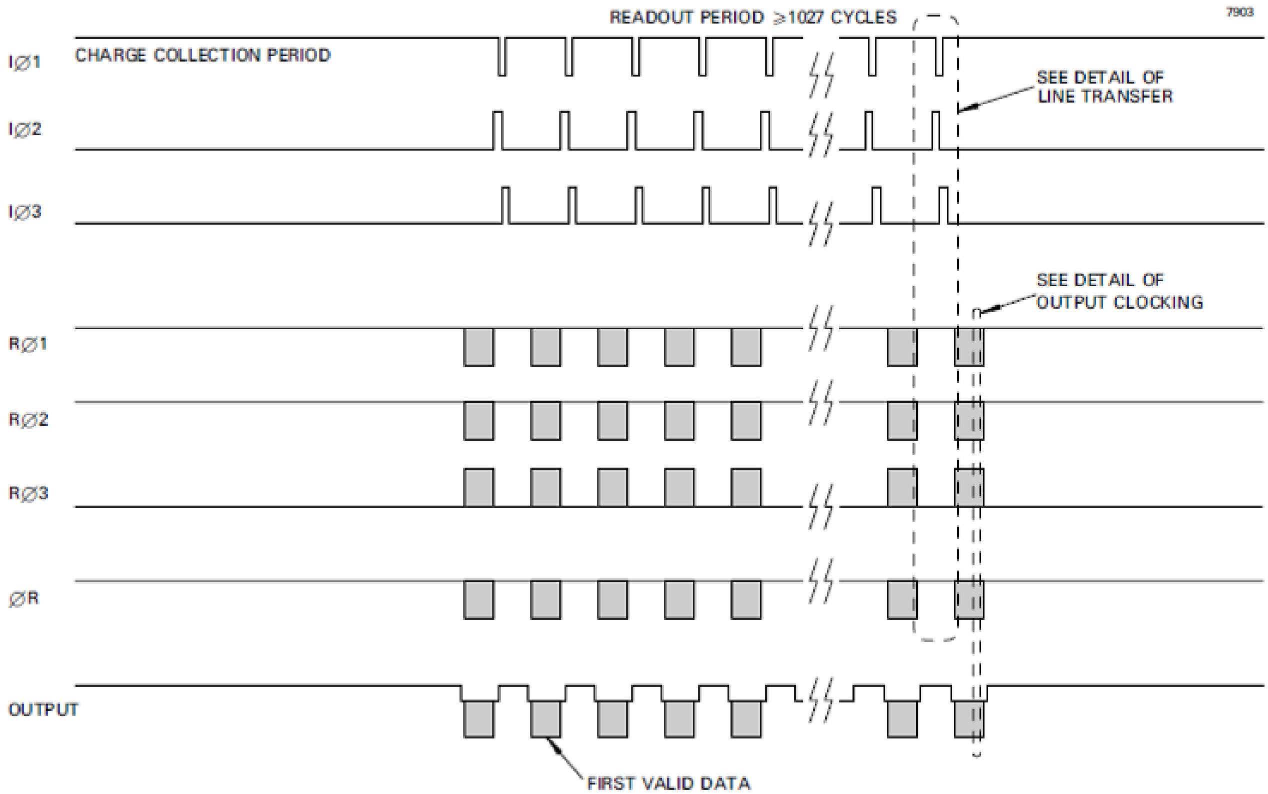
	Typical	Units
I∅/I∅ inter-phase	1.5	nF
I∅/SS	5	nF
R∅/R∅ inter-phase	40	pF
R∅/SS	150	pF
R∅/(SS+DG+OD)	10	pF
Output impedance	300	Ω

AIMO

	Typical	Units
I∅/I∅ inter-phase	3.5	nF
I∅/SS	4.5	nF
R∅/R∅ inter-phase	40	pF
R∅/SS	10	pF
R∅/(SS+DG+OD)	60	pF
Output impedance	300	Ω

FRAME READOUT TIMING DIAGRAM

NIMO

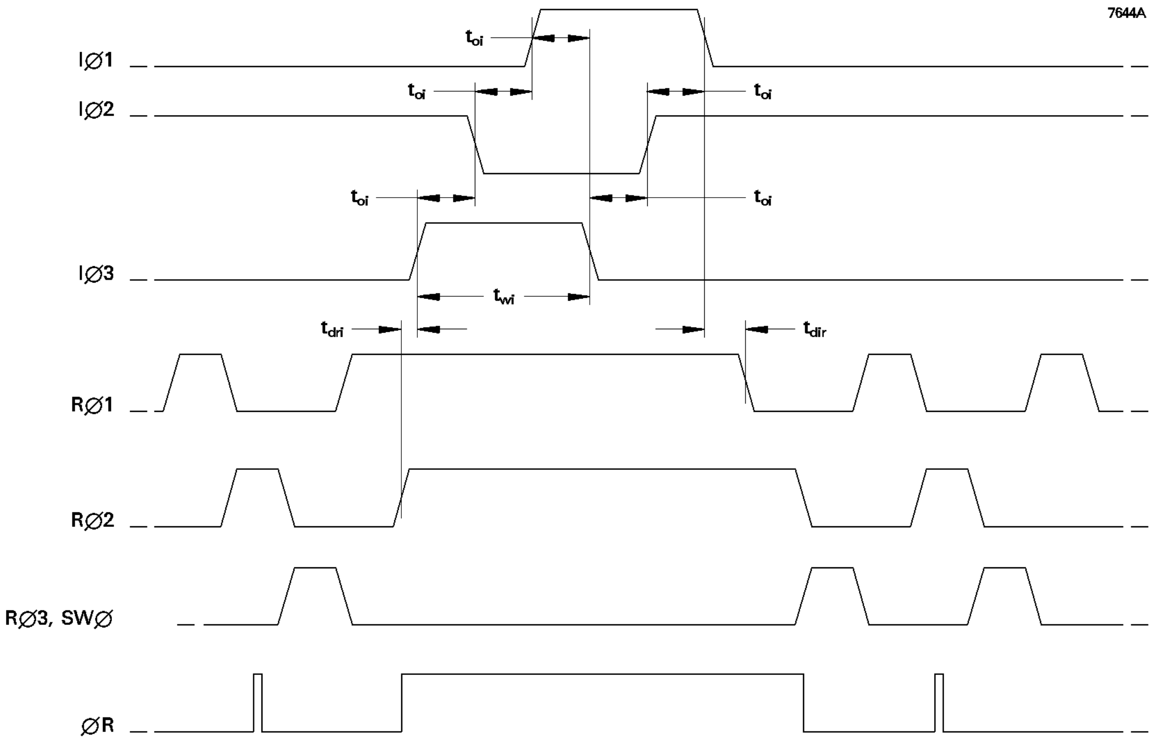


AIMO

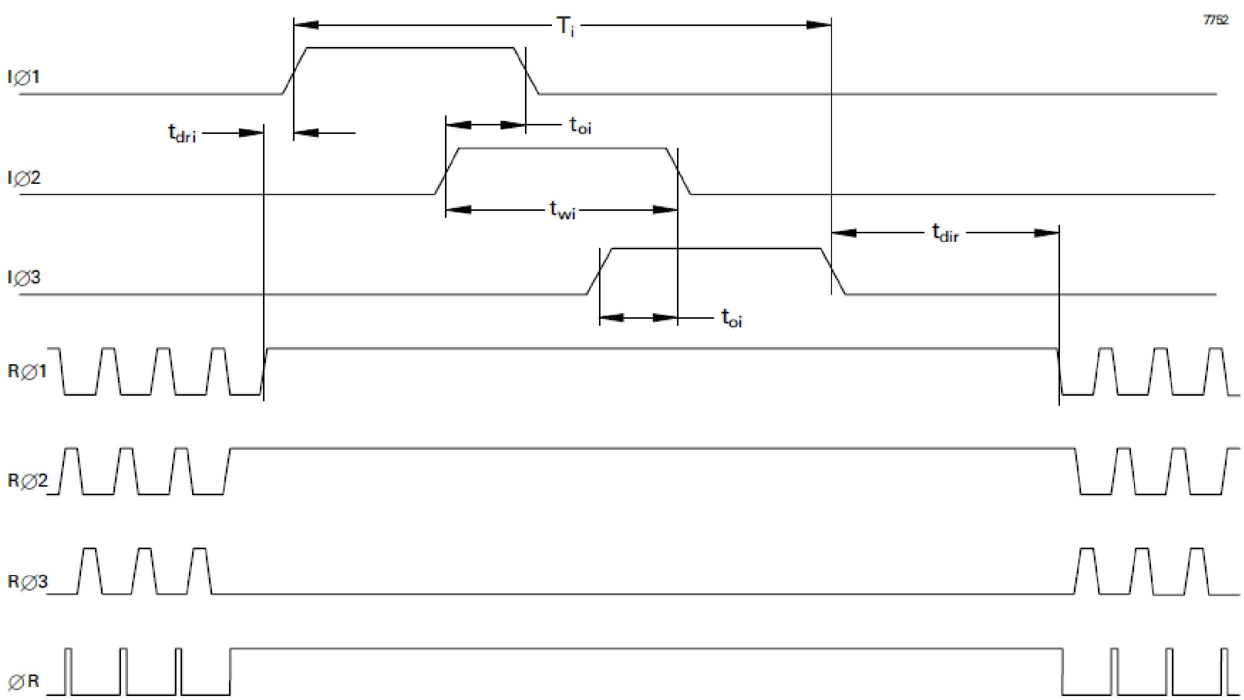
See detail in line transfer and output clocking sections.

DETAIL OF LINE TRANSFER (For output from single amplifier)

NIMO

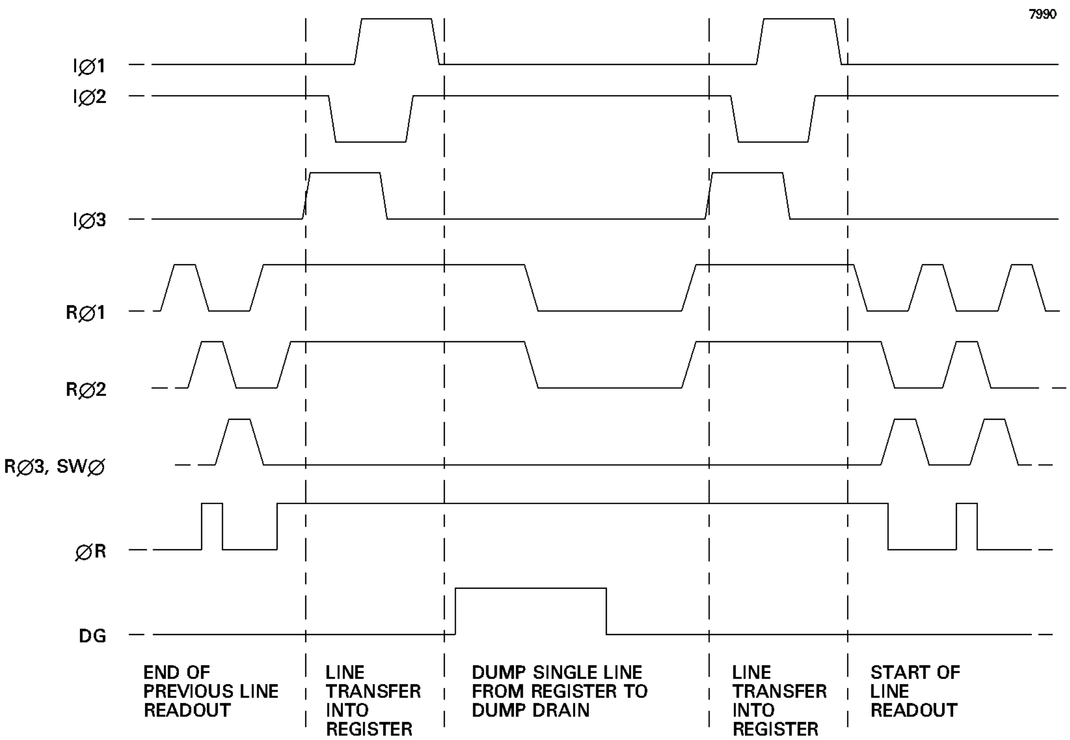


AIMO

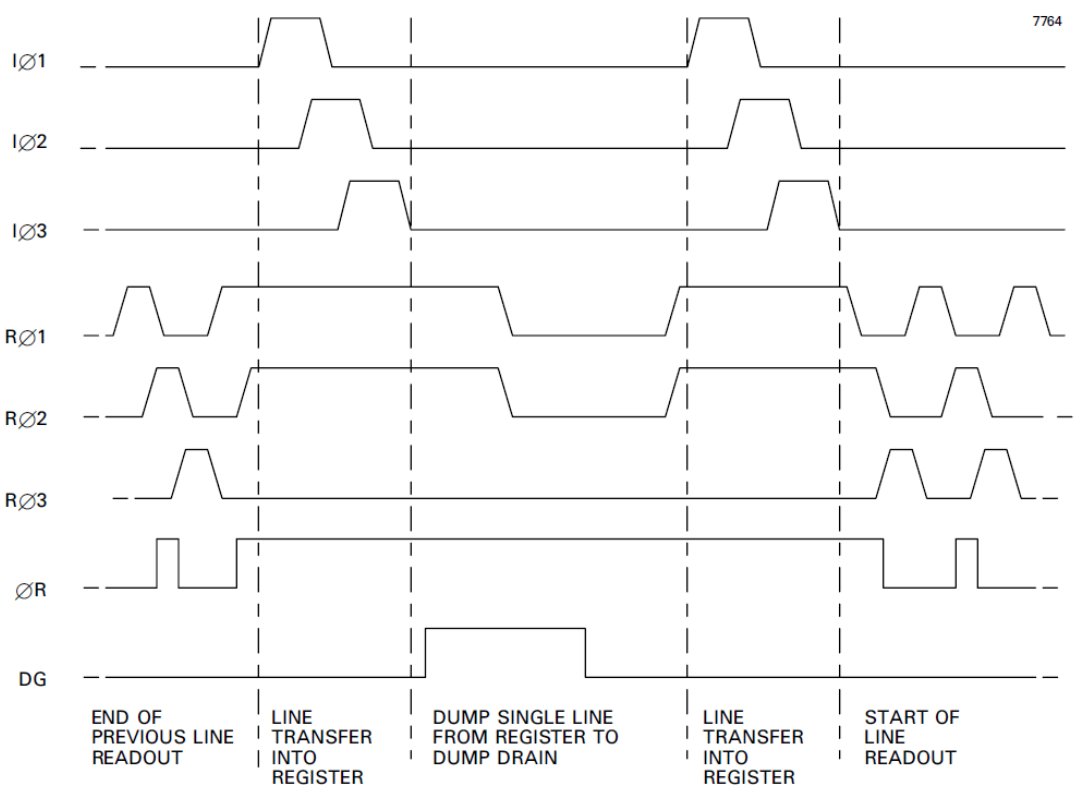


DETAIL OF VERTICAL LINE TRANSFER (Single line dump)

NIMO

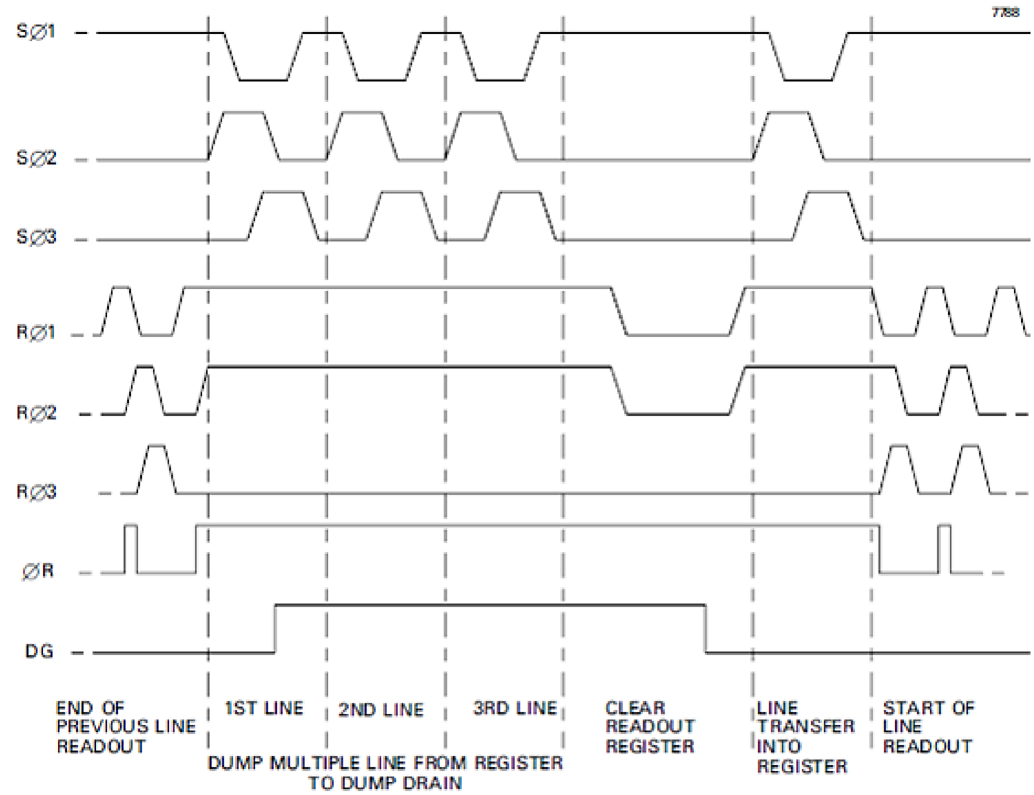


AIMO

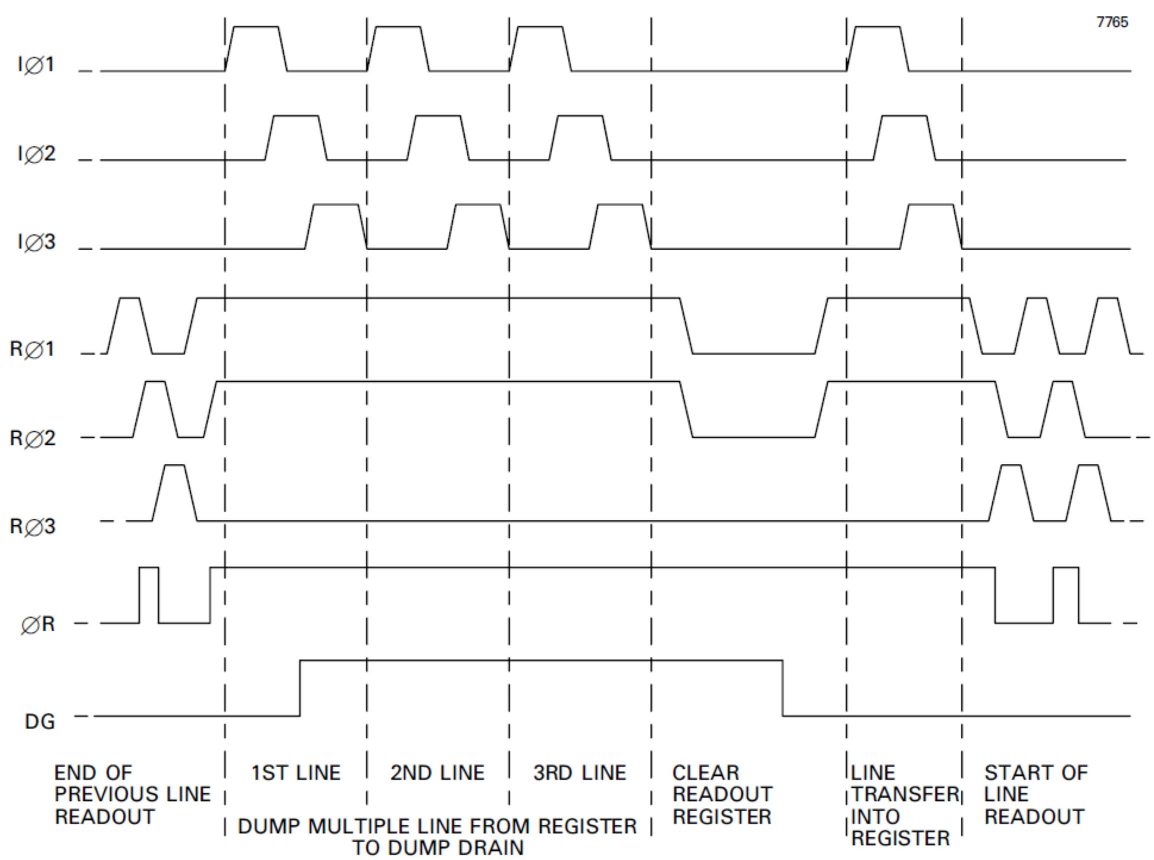


DETAIL OF VERTICAL LINE TRANSFER (Multiple line dump)

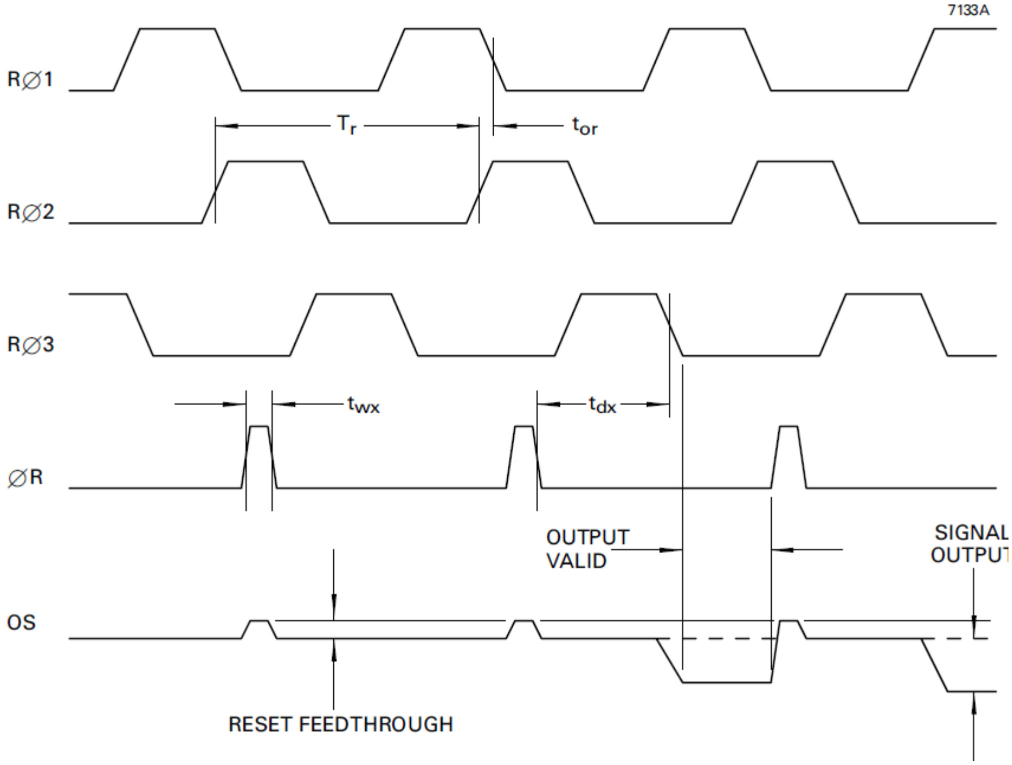
NIMO



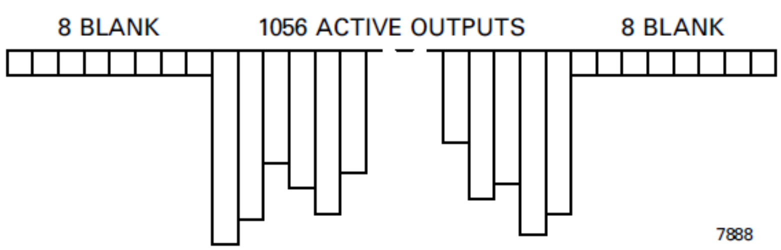
AIMO



DETAIL OF OUTPUT CLOCKING (Operation through both outputs)



LINE OUTPUT FORMAT



CLOCK TIMING REQUIREMENTS

NIMO

Symbol	Description	Min	Typical	Max	Units
T_i	Image clock period	4	14	see note 20	μs
t_{wi}	Image clock pulse width	2	5	see note 20	μs
t_{ri}	Image clock pulse rise time (10 to 90%)	0.1	5	$T_i – 2t_{wi}$	μs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	t_{ri}	$T_i – 2t_{wi}$	μs
t_{oi}	Image clock pulse overlap	$(t_{ri} + t_{fi}) / 2$	0.6	$(3t_{wi} - T_i) / 2$	μs
t_{dir}	Delay time, I∅ stop to R∅ start	1	2	see note 20	μs
t_{dri}	Delay time, R∅ stop to I∅ start	1	1	see note 20	μs
T_r	Output register clock cycle period	200	1000	see note 20	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.3T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	$0.2t_{wx}$	$0.5t_{rr}$	$0.1T_r$	ns
t_{dx}	Delay time, ∅R low to R∅3 low	30	$0.5T_r$	$0.8T_r$	ns

AIMO

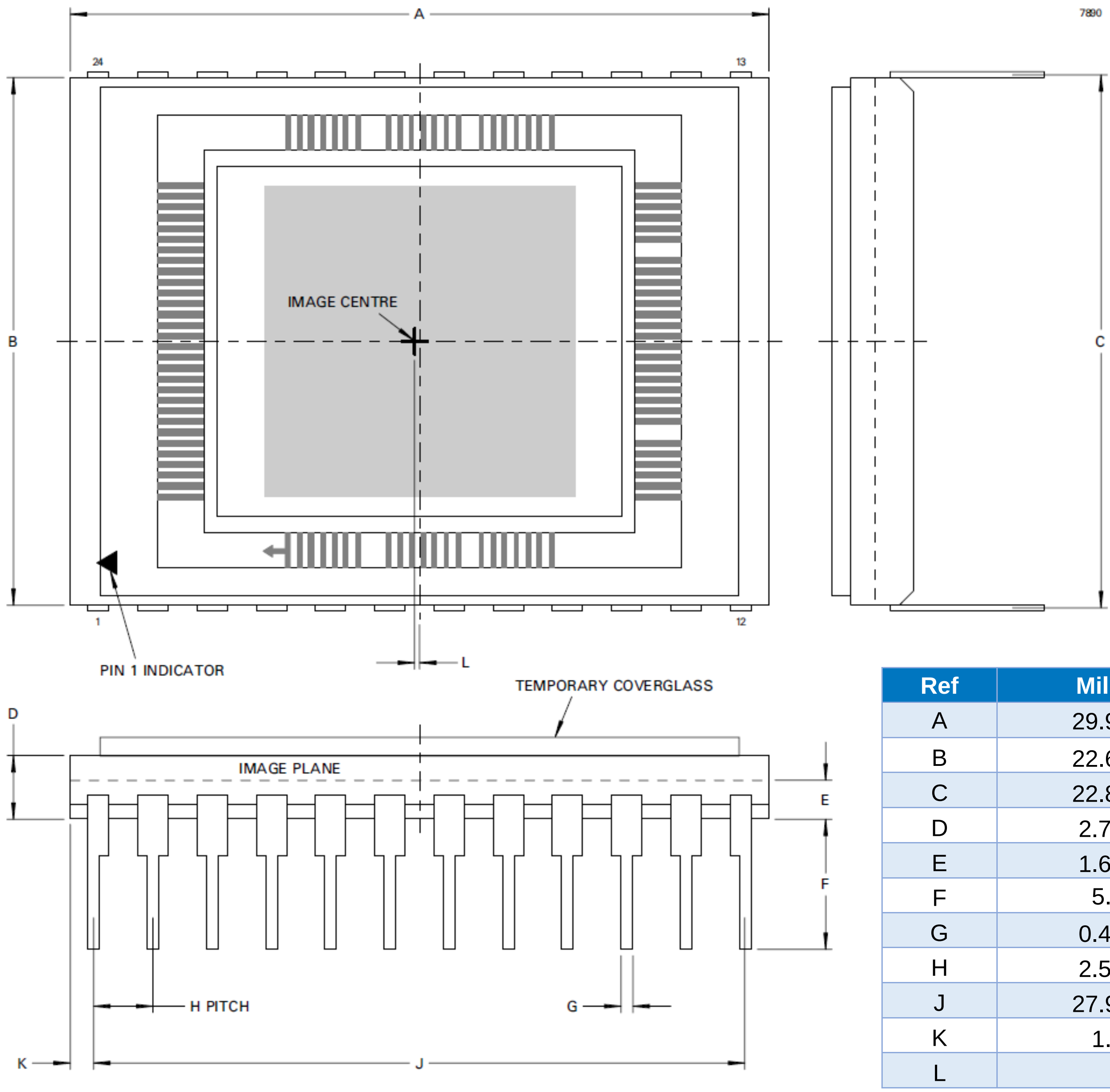
Symbol	Description	Min	Typical	Max	Units
T_i	Image clock period	50	100	see note 20	μs
t_{wi}	Image clock pulse width	25	50	see note 20	μs
t_{ri}	Image clock pulse rise time (10 to 90%)	0.1	5	$T_i – 2t_{wi}$	μs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	t_{ri}	$T_i – 2t_{wi}$	μs
t_{oi}	Image clock pulse overlap	$(t_{ri} + t_{fi}) / 2$	5	$(3t_{wi} - T_i) / 2$	μs
t_{dir}	Delay time, I∅ stop to R∅ start	1	2	see note 20	μs
t_{dri}	Delay time, R∅ stop to I∅ start	1	1	see note 20	μs
T_r	Output register clock cycle period	200	1000	see note 20	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.3T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	$0.2t_{wx}$	$0.5t_{rr}$	$0.1T_r$	ns
t_{dx}	Delay time, ∅R low to R∅3 low	30	$0.5T_r$	$0.8T_r$	ns

NOTES

20. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.

PACKAGE DETAIL

All dimensions shown in mm. Dimensions without limits are nominal. Contact Teledyne e2v for further package details.



Ref	Millimeters
A	29.94 ± 0.30
B	22.61 ± 0.25
C	22.86 ± 0.25
D	2.70 ± 0.27
E	1.65 ± 0.25
F	5.6 ± 0.5
G	0.46 ± 0.05
H	2.54 ± 0.13
J	27.94 ± 0.13
K	1.0 ± 0.3
L	0.2

HEALTH AND SAFETY HAZARDS

Teledyne e2v devices are safe to handle and operate, provided that the relevant precautions stated herein are observed. Teledyne e2v does not accept responsibility for damage or injury resulting from the use of devices it produces. Equipment manufacturers and users must ensure that adequate precautions are taken. Appropriate warning labels and notices must be provided on equipment incorporating Teledyne e2v devices and in operating manuals.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (pins 2, 3, 4, 6, 7, 8, 9, 12, 19) but not to the other pins.

The devices are assembled in a clean room environment. Teledyne e2v recommend that similar precautions are taken to avoid contaminating the active surface.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to an ionising radiation. Users planning to use CCDs in a high radiation environment are advised to contact Teledyne e2v.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	153	-	373	K
Operating	153	233	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling............. 5 K/min

PART REFERENCES

Variant	Operating Mode	Illumination	Enhanced BSI Process	Silicon	AR Coating	Fringe Suppression
CCD47-10-G-109	NIMO	BSI	No	Deep Depletion	NIR	Yes
CCD47-10-G-197	NIMO	BSI	Yes	Deep Depletion	ML2	Yes
CCD47-10-G-768	NIMO	BSI	No	Deep Depletion	None	Yes
CCD47-10-G-174 (See note 9)	NIMO	BSI	Yes	Standard	UV	No
CCD47-10-G-353	AIMO	BSI	No	Standard	Midband	No
CCD47-10-G-355	AIMO	BSI	No	Standard	None	No
CCD47-10-G-112	AIMO	BSI	Yes	Standard	None	No
CCD47-10-G-373	AIMO	BSI	Yes	Standard	UV	No
CCD47-10-G-S55	AIMO	BSI	Yes	Standard	Broadband	No

Grade Definitions

Grade 0	Super Grade	Meets all Grade 0 performance parameters and cosmetic parameters
Grade 1	Science Grade	Meets all Grade 1 performance parameters and cosmetic parameters
Grade 5	Engineering Grade	Electrically functional with no performance or cosmetic parameter guarantees
Grade 6	Mechanical Grade	Non-functional. Mechanically representative only.

NOTES

21. G = Grade (e.g. 1)
22. Additional variants may be available to custom order. Consult Teledyne e2v for more information.