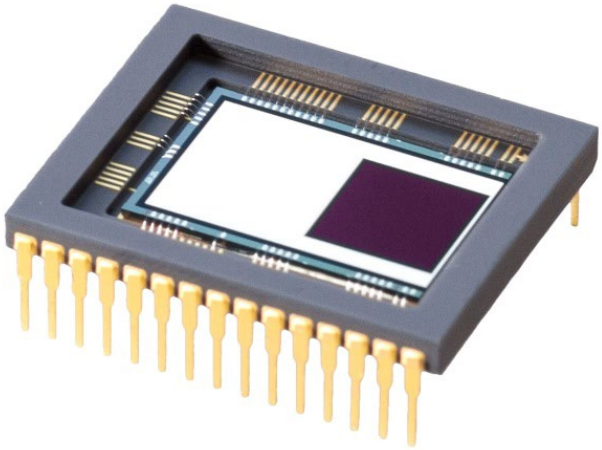
CCD97-00

512 x 512 BSI EMCCD



KEY FEATURES

- 512 x 512 active pixels
- 16µm square pixels
- Single photon sensitive
- Variable multiplicative gain
- Additional conventional output amplifier
- Frame Transfer
- Inverted mode operation for low dark current
- 30-pin ceramic dual-in-line package

TYPICAL APPLICATIONS

- Advanced Microscopy
- Fast Astronomy
- Quantum Imaging

PART REFERENCES

Please see last page for full list of available parts.

GENERAL DATA

Format	
Image Area	8.19 mm x 8.19 mm
Active Pixels	512 x 512 (note 1)
Pixel Size	16 µm x 16 µm
Number of output amplifiers	2 (Electron multiplying and Conventional)
Package	
Package Size	22.86 x 28.00 mm
Number of pins	30
Window	Removable Glass
Performance	
Typical Amplifier Responsivity	5.3 µV/e^- (OSH) 1.1 µV/e^- (OSL)
Typical Readout Noise	<1e^- at 1MHz at 1000x Gain 3.1e^- at 50kHz using OSH amp.
Max Output data rate	15MHz
Typical pixel charge capacity	130 ke^-/pixel
Typical dark signal (20°C)	400 e^-/pixel/s

OVERVIEW

The CCD97 is a frame transfer, electron multiplying CCD sensor designed for extreme performance in high frame rate ultra-low light applications. The Teledyne e2v back-thinning process ensures high quantum efficiency over a wide range of wavelengths.

An electron multiplying CCD functions by having an extended readout register with variable gain from 1x to 1000x prior to voltage conversion in the output amplifier. This allows readout noise to be effectively eliminated while maintaining fast readout rates.

The device can also be read out without using the gain register via the High Responsivity Output amplifier (OSH) for high dynamic range.

The gain may be varied from 1x to over 1000x by adjustment of the multiplication phase amplitude RØ2HV

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PERFORMANCE

Except where otherwise specified, the following are measured at 18°C at a pixel rate of 11 MHz, with typical operating voltages. For the S28 variant, the parameters relating to the OSH amplifier do not apply; all other parameters are unchanged.

Parameter	Min	Typical	Max	Units	Notes
Output amplifier responsivity, OSH amplifier	-	5.3	-	µV/e⁻	2
Output amplifier responsivity, OSL amplifier	-	1.1	-	µV/e⁻	2, 3
Multiplication register gain, OSL amplifier	1	-	1000		4
Peak signal - 2-phase IMO	90k	150k	-	e⁻/pixel	5
Charge handling capacity of multiplication register	-	800k	-	e⁻/pixel	6
Readout noise at 50 kHz with CDS, OSH amplifier	-	2.2	-	e⁻ rms	7
Readout noise at 1 MHz with CDS, OSH amplifier	-	5.4	-	e⁻ rms	7
Amplifier reset noise (without CDS), OSH amplifier	-	50	-	e⁻ rms	7
Readout noise at 50 kHz with CDS, OSL amplifier	-	6	-	e⁻ rms	3, 7
Readout noise at 15 MHz with CDS, OSL amplifier	-	14	-	e⁻ rms	3, 7
Amplifier reset noise (without CDS), OSL amplifier	-	120	-	e⁻ rms	3, 7
Readout noise at 1 MHz and 1000X gain	-	<1	-	e⁻ rms	7
Maximum frequency (settling to 1%), OSH amplifier	-	-	3	MHz	7, 8
Maximum frequency (settling to 5%), OSH amplifier	-	-	4.5	MHz	7, 8
Maximum frequency (settling to 1%), OSL amplifier	-	-	9	MHz	7, 8
Maximum frequency (settling to 5%), OSL amplifier	-	-	15	MHz	7, 8
Maximum parallel transfer frequency	-	1.6	-	MHz	2
Dark signal equivalent at 20°C	-	400	800	e⁻/pixel/s	9, 10
Dark signal non-uniformity (DSNU) equivalent at 20°C	-	60	-	e⁻/pixel/s	11
Excess noise factor	-	√2	-		12

NOTES

1. For the Multi-19 variant a reduced format of 506 x 506 is recommended due to reduced responsivity at the edges of the image area.
2. Measured at a pixel rate of 1 MHz.
3. No EM gain applied.
4. Some increase of RØ2HV may be required throughout life to maintain gain performance.
5. For Multi-2 and Multi-19 variants, the peak signal is 95k e⁻ typical and 75k e⁻ min.
6. When multiplicative gain is used, a linear response is achieved for output signals up to 400 ke⁻.
7. Values are inferred from design.
8. The quoted maximum frequencies assume a 20 pF load and correlated double sampling (CDS) are being implemented. If instead a single sampling is used, the output will be settled to 1% at 15 MHz typically.

   The quoted dark signal has the usual temperature dependence for inverted mode operation. For operation at high frame rates with short integration times, there will also be a significant component generated during readout through the non-inverted mode register.
9. There exists a further weakly temperature dependant component, the clock induced charge (CIC), which is independent of integration time. For more information, refer to the technical note "Dark Signal and Clock-Induced Charge in L3Vision™ CCD Sensors".
10. For fringe suppression variants, the dark signal will be higher (typical and maximum are 600 and 900 e⁻/pixel/s respectively).
11. DSNU is defined as the 1σ variation of the dark signal.
12. The excess noise factor is defined as the factor by which the multiplication process increases the shot noise on the image when multiplication gain is used.

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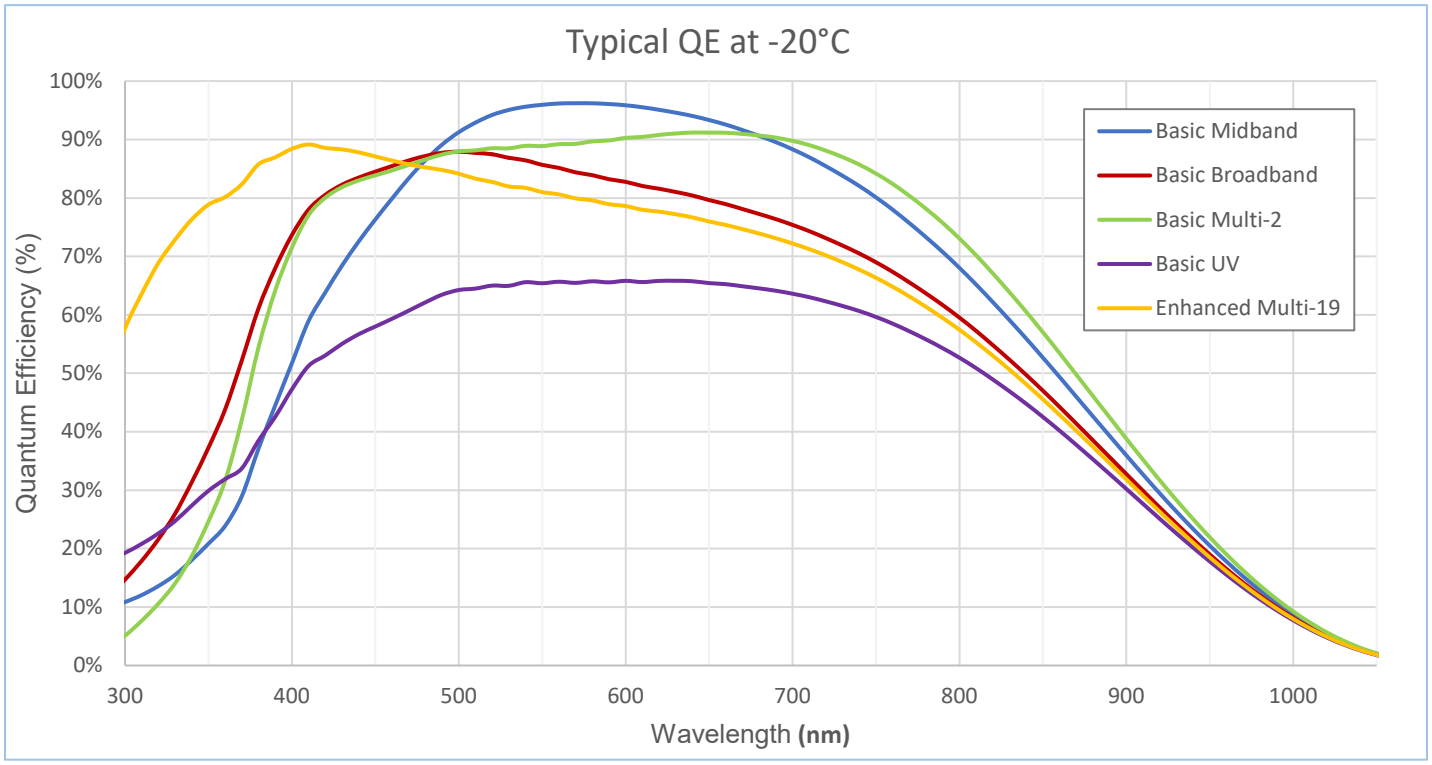
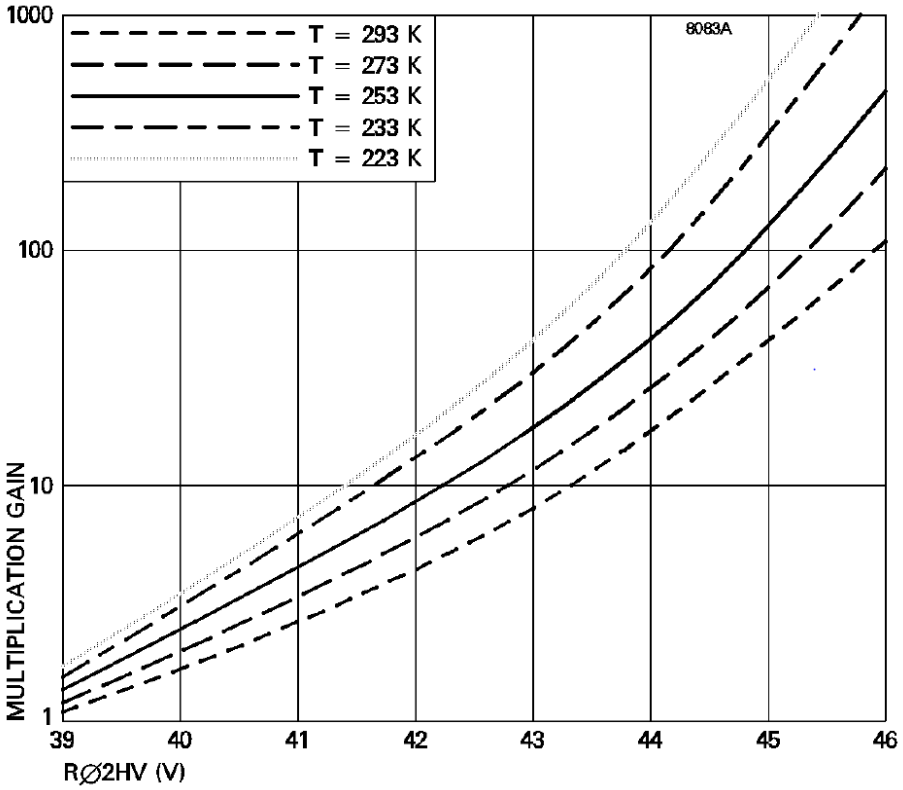
SPECTRAL RESPONSE



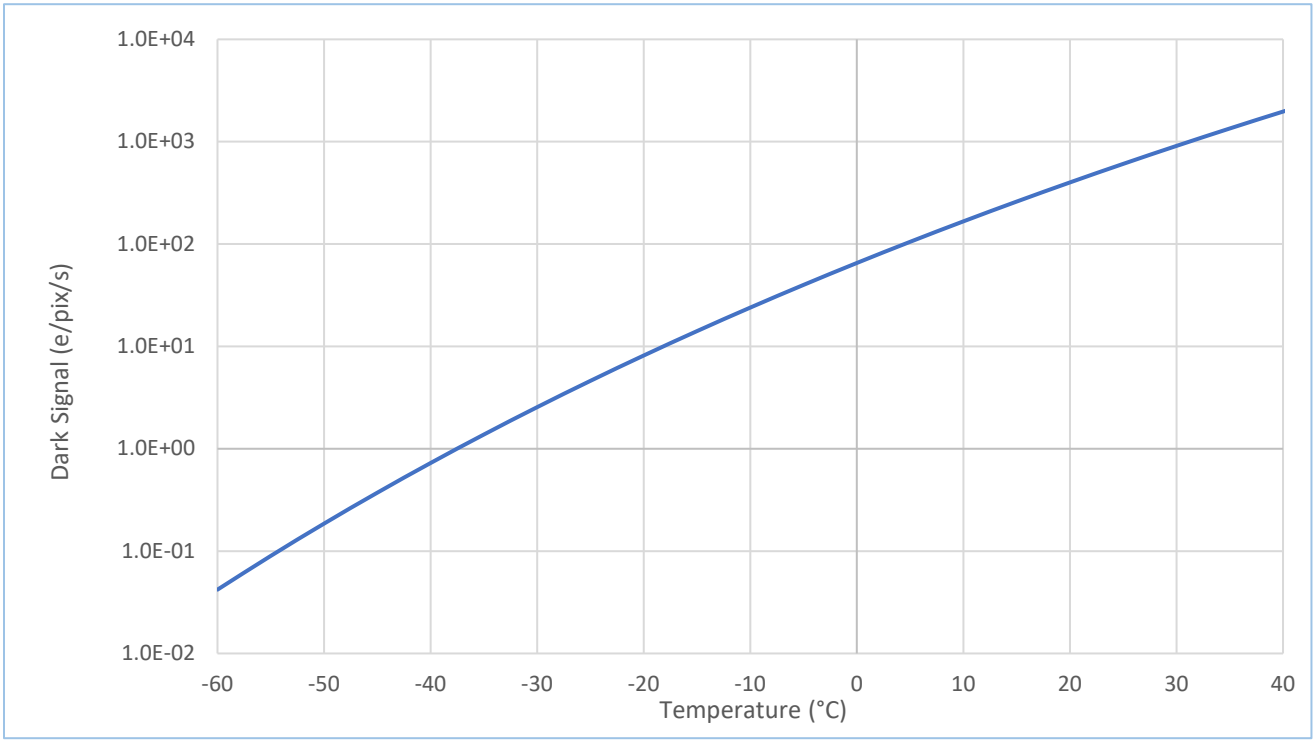
Devices can be supplied with alternative anti-reflection coatings optimised for different wavelengths – details from Teledyne e2v.

TYPICAL VARIATION OF MULTIPLICATIVE GAIN WITH RØ2HV MINUS RØDC



TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE

Dark signal is a strong function of temperature and the typical average (background) dark signal at any temperature T (kelvin) between 150 K and 300 K is given by $Q_d/Q_{do} = 1.14 \times 10^6 T^3 e^{-9080/T}$ where Q_{do} is the dark current at 293 K.



COSMETIC SPECIFICATION

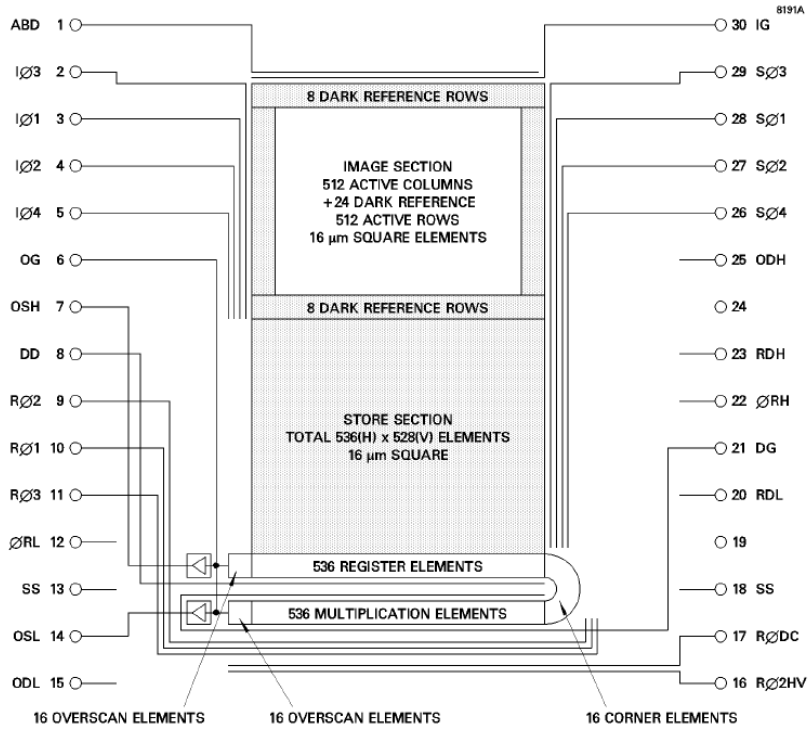
All cosmetic tests are performed at 18 ± 3ºC in 2-phase inverted mode at 11MHz.

Grade	1
White Defects	10
White Columns	0
Black/Pin-head Columns	0

Cosmetic definitions

White Defects	White defects are pixels having a dark signal generation rate corresponding to an output signal of greater than 5 times the maximum dark signal level.
White Columns	A white column contains at least 9 white defects.
Black/Pin-head Columns	Black defects are counted when they have a responsivity of less than 80% of the local mean signal at approximately the specified gain and level of illumination. A black column contains at least 9 black defects. Pin-head columns are manifest as a partial dark column with a bright pixel showing photo-response at the end of the column nearest to the readout register. Pin-head columns are counted when the black column has a responsivity of less than 80% of the local mean signal at approximately the specified multiplication gain and level of illumination. A pin-head column contains at least 9 black defects.

DEVICE ARCHITECTURE



The rows and colums immediately adjacent to the active image area may be only partially shielded, i.e. transition elements, and should not be used for reference purposes.

The electrodes of the image and store sections are configured for four-phase clocking, but adjacent phases need to be joined off chip to run in two phase operation.

The multiplication register requires two extra drive phases, RØDC and RØ2HV.

There is a dump drain DD below the 536 register elements adjacent to the store section with the charge dumping operation controlled by the dump gate DG.

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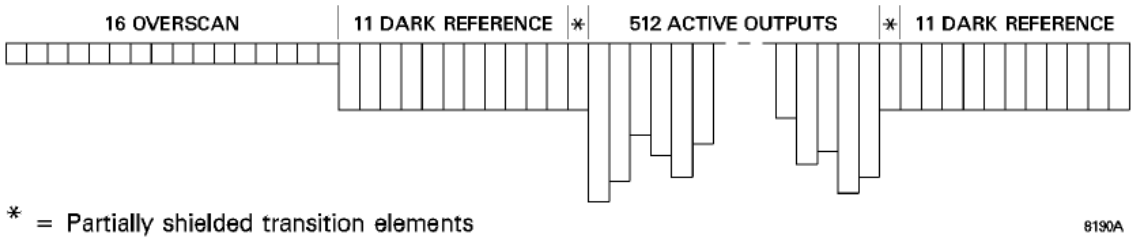
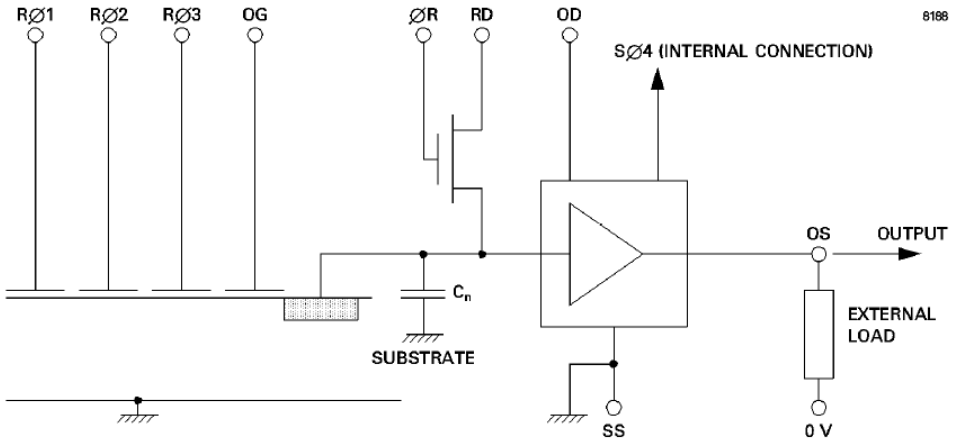
LINE OUTPUT FORMAT



NOTES

13. there will be a one row propagation delay between transferring a row from the store section to the conventional register and then reading it out through the OSL CCD output.

OUTPUT CIRCUIT



The amplifiers have a DC restoration circuit that is internally activated whenever SØ4 is high.

Nominal Design Features (Not measured)

Feature	OSH	OSL
Output	OSH (pin 7)	OSL (pin 14)
External load	5 kΩ or 5 mA	5 kΩ or 5 mA
Output impedance	250 Ω	350 Ω
On-chip dissipation	30 mW	40 mW

CONNECTIONS TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

Pin	Ref	Function	MIN (V)	MAX (V)
1	ABD	Anti-blooming drain	-0.3	+25
2	IØ3	Image section clock phase 3	-20	+20
3	IØ1	Image section clock phase 1	-20	+20
4	IØ2	Image section clock phase 2	-20	+20
5	IØ4	Image section clock phase 4	-20	+20
6	OG	Output gate	-20	+20
7	OSH (note 14)	Output source high	-0.3	+25
8	DD	Dump drain	-0.3	+25
9	RØ2	Register clock phase 2	-20	+20
10	RØ1	Register clock phase 1	-20	+20
11	RØ3	Register clock phase 3	-20	+20
12	ØRL	Output reset pulse low	-20	+20
13	SS	Substrate	0	
14	OSL	Output source low	-0.3	+25
15	ODL	Output drain low	-0.3	+32
16	RØ2HV	Register clock phase 2 HV	-20	+50
17	RØDC	Register DC phase	-20	+20
18	SS	Substrate	0	
19	n.c.	No connection	-	
20	RDL	Reset drain low	-0.3	+25
21	DG	Dump gate	-20	+20
22	ØR	Output reset pulse high	-20	+20
23	RDH	Reset drain high	-0.3	+25
24	n.c.	No connection	-	
25	ODH	Output drain high	-0.3	+25
26	SØ4	Store section clock phase 4	-20	+20
27	SØ2	Store section clock phase 2	-20	+20
28	SØ1	Store section clock phase 1	-20	+20
29	SØ3	Store section clock phase 3	-20	+20
30	IG	Isolation gate	-20	+20

14. Pin 7 is n.c. no connection for S28 variant. The ABD pin is used for connection purposes and must be biased as specified even for non-anti-blooming variants.

MAXIMUM VOLTAGE BETWEEN PAIRS

Pin	Ref	Pin	Ref	Min (V)	Max (V)
7	OSH	**25**	ODH	-15	+15
14	OSL	**15**	ODL	-15	+15
16	RØ2HV	**17**	RØDC	-20	+50
16	RØ2HV	**11**	RØ3	-20	+50
Output Transistor Current (mA)					20

OPERATING VOLTAGES

Typical operating voltages are as given in the table below. Some adjustment within the minimum-maximum range specified may be required to optimise performance.

Connection	Description	Phase Amplitude or DC level (V)			Notes
		Min	Typical	Max	
IØ1, 2, 3, 4 high	Image section: clock high	+5	+7	+9	15
IØ1, 2, 3, 4 low	Image section: clock low	-6	-5	-4	
SØ1, 2, 3, 4 high	Store section: clock high	+5	+7	+9	15
SØ1, 2, 3, 4 low	Store section: clock low	-6	-5	-4	
RØ1, 2, 3 high	Register: clock high	+8	+12	+13	
RØ1, 2, 3 low	Register: clock low	-	0	-	
RØ2HV high	Register HV phase high	+20	+40	+50	5
RØ2HV low	Register HV phase low	0	+4	+5	
ØR high	Reset clock high	-	+10	-	16
ØR low	Reset clock low	-	0	-	
RØDC	Register DC phase	+2	+3	+5	
OG	Output gate voltage	+1	+3	+5	17
IG	Isolation gate voltage	-	-5	-	
SS	Substrate	0	+4.5	+7	
ODL, ODH	Output drain	+25	+28	+32	
RD	Reset drain voltage	+15	+17	+20	
ABD	Anti-blooming Drain	+10	+18	+20	
DG high	Dump gate high	-	0	-	
DG low	Dump gate low	+10	+12	+13	
DD	Dump drain	+20	+24	+25	

NOTES

15. IØ and SØ adjustment may be common. The high level may need to be adjusted to achieve correct charge transfer and the low level may need to be separately adjusted to achieve correct inverted mode operation that is uniform across the array. Alternatively, adjustment of SS with IØ and SØ low levels fixed at the nominal values can be used to achieve the same result.
16. ØRL and ØRH high level may be adjusted in common with RØ1, 2, 3.
17. Other than the output gates (OG), there are no common connections made between the two amplifiers, and either can be powered down by connecting the appropriate output drain (OD) connection to the substrate (SS). The reset drains (RD) should remain biased, with the reset gate (ØR) clocked normally or held at clock low level.

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ELECTRICAL INTERFACE CHARACTERISTICS (not measured)

ELECTRODE CAPACITANCES AT MID CLOCK LEVELS					SERIES RESISTANCES	
Connection	To SS	Inter-phase	Total	Units	Total	Units
IØ1	3.7	1.6	5.3	nF	17	Ω
IØ2	1.6	1.6	3.2	nF	17	Ω
IØ3	3.7	1.6	5.3	nF	17	Ω
IØ4	1.6	1.6	3.2	nF	17	Ω
SØ1	3.7	1.6	5.3	nF	17	Ω
SØ2	1.6	1.6	3.2	nF	17	Ω
SØ3	3.7	1.6	5.3	nF	17	Ω
SØ4	1.6	1.6	3.2	nF	17	Ω
RØ1	50	65	115	pF	6	Ω
RØ2	32	43	75	pF	6	Ω
RØ3	62	63	125	pF	6	Ω
RØ2HV	28	37	65	pF	2	Ω

CLOCK TIMING REQUIREMENTS

The device is of a 4-phase construction, designed to operate in 2-phase inverted mode. This is achieved by applying common timings to phases Ø1 and Ø2, and phases Ø3 and Ø4 of the image and store sections. Suggested timing diagrams are shown in Figs. 4-11.

The following are suggested pulse rise and fall times:

Clock Pulse	Typical Rise Time τ (ns)	Typical Fall Time τ (ns)	Typical Pulse Overlap
IØ	120 < τ <200	120 < τ <200	@90% points
SØ	120 < τ <200	120 < τ <200	@90% points
RØ1	10	10	@70% points
RØ2	10	10	@70% points
RØ3	10	10	@70% points
RØ2HV	25	25	See 18
RØ2HV	Sine	Sine	Sinusoid – high on falling edge of RØ1

NOTES

18. RØ2HV can be operated with a normal clock pulse, as shown in Fig. 6. Alternatively, a sinusoidal clocking scheme is shown in Fig. 5. The requirement for successful clocking is that RØ2HV reaches its maximum amplitude before RØ1 goes low.

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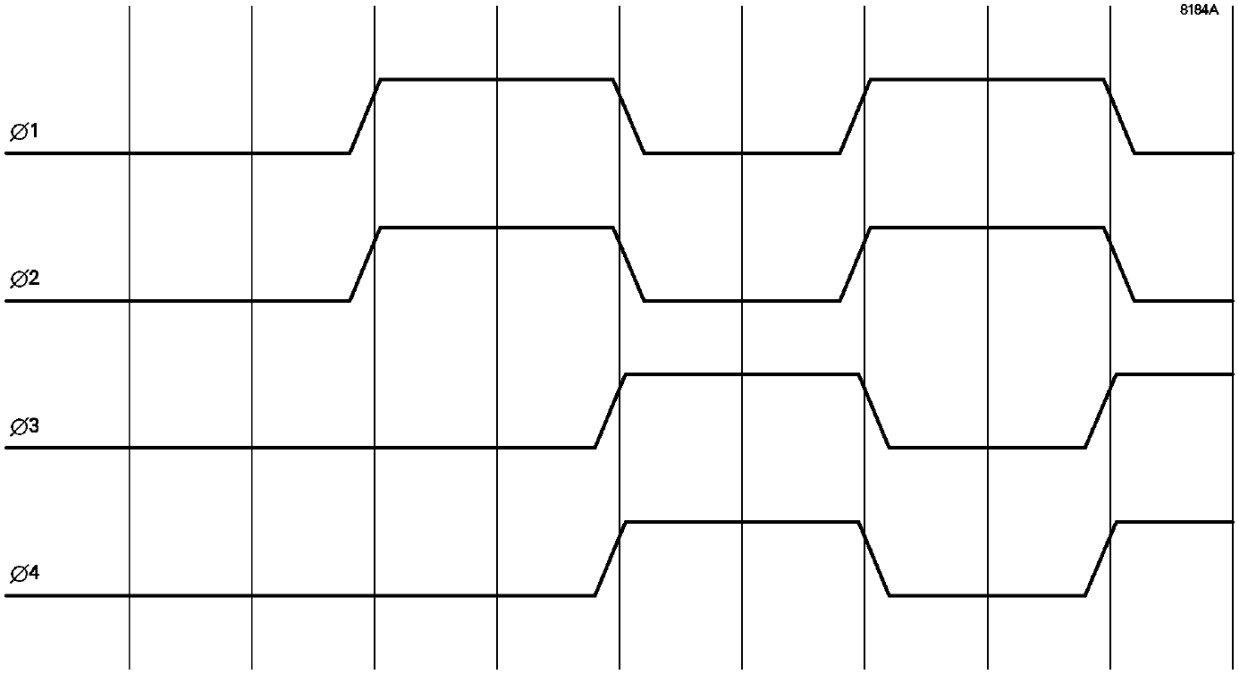
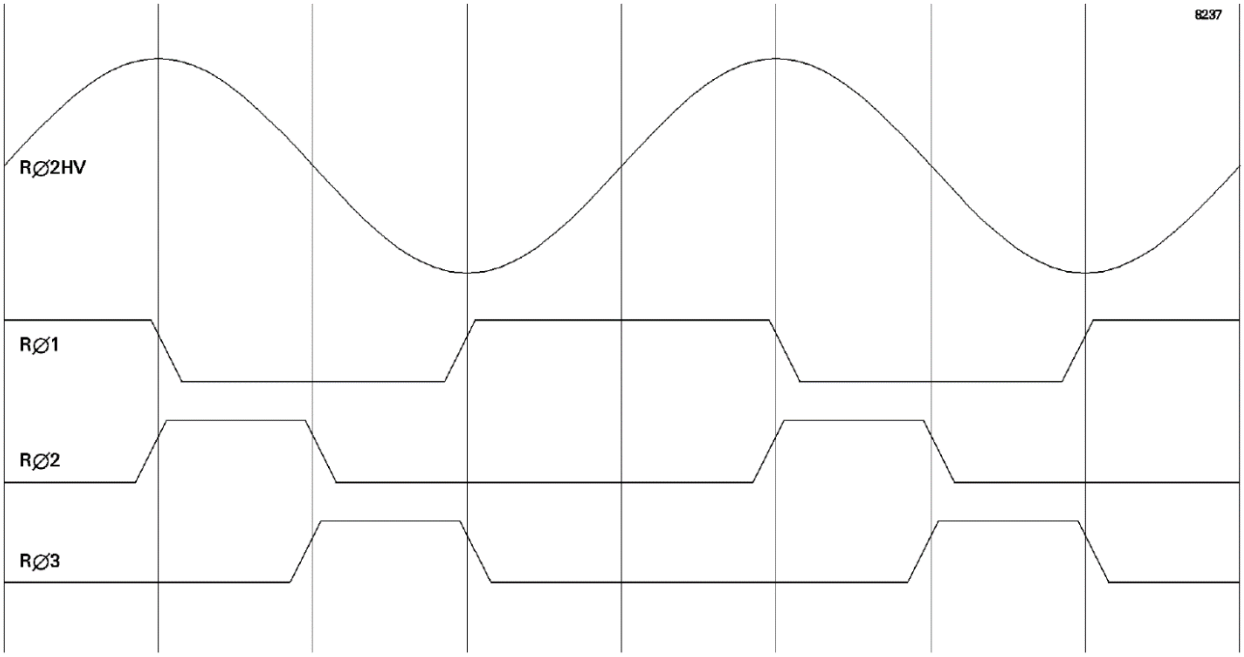
CLOCKING SCHEME FOR 2-PHASE INVERTED MODE OPERATION



CLOCKING SCHEME FOR MULTIPLICATION GAIN

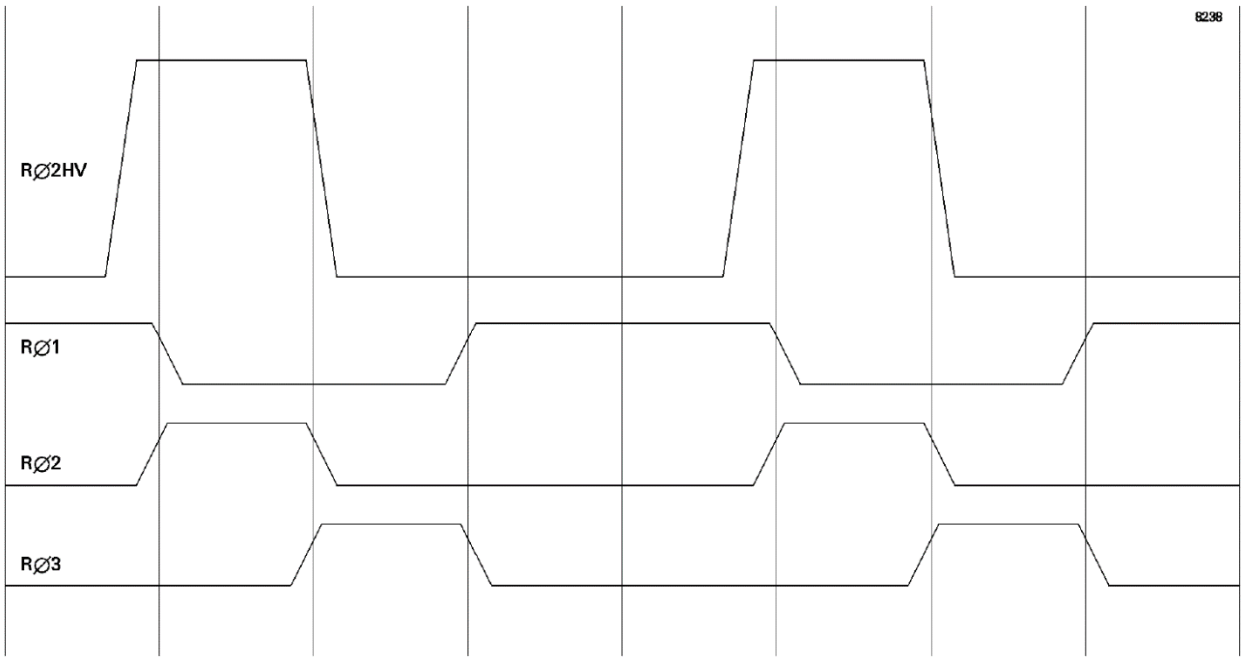
Sinusoidal Clocking Scheme

See note 19, used for factory testing



Trapezoidal Clocking Scheme

See note 19, not used in factory testing

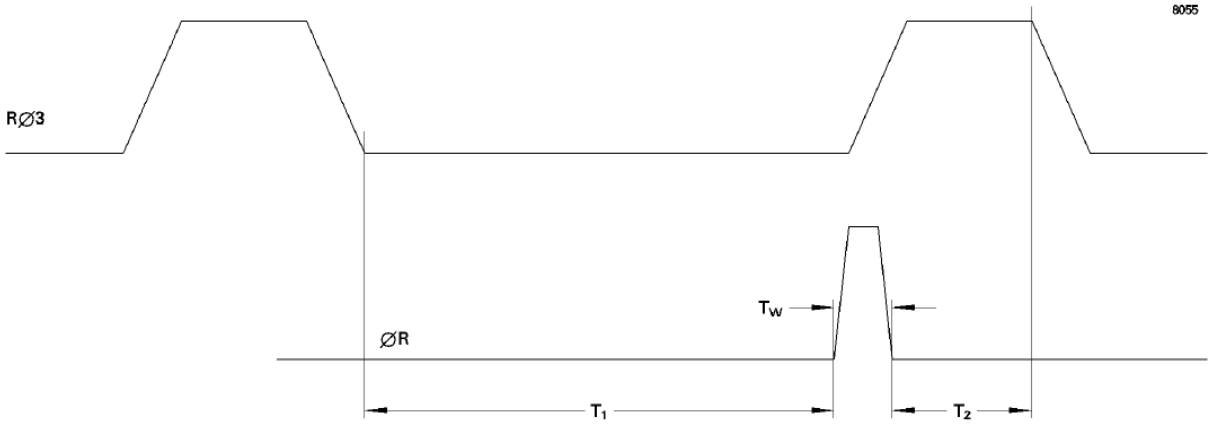


NOTES

19. To operate through the OSH output amplifier, the RØ1 and RØ2 waveforms should be interchanged.

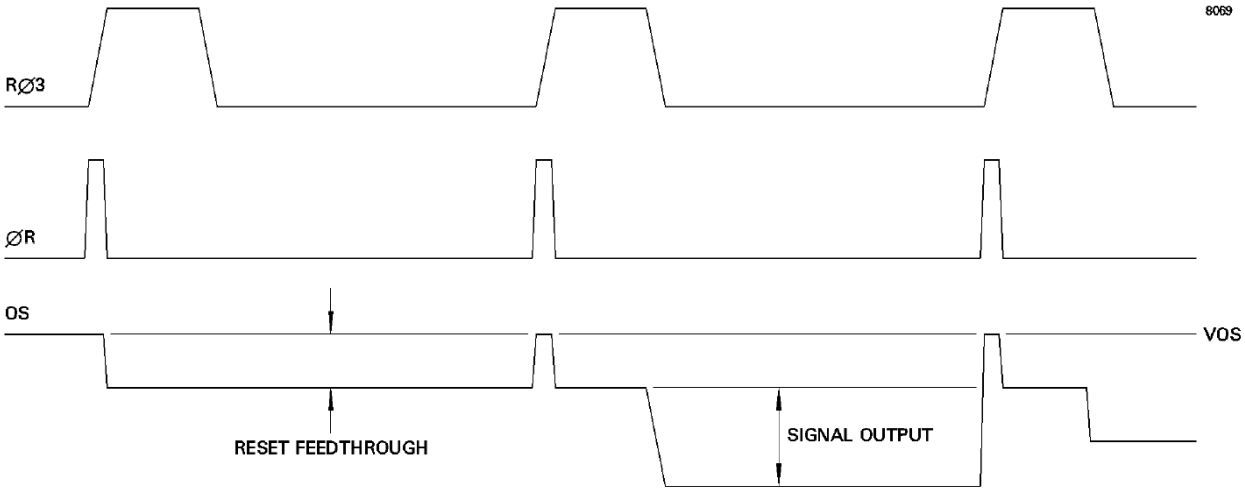
PULSE TIMINGS AND OVERLAPS

Reset Pulse

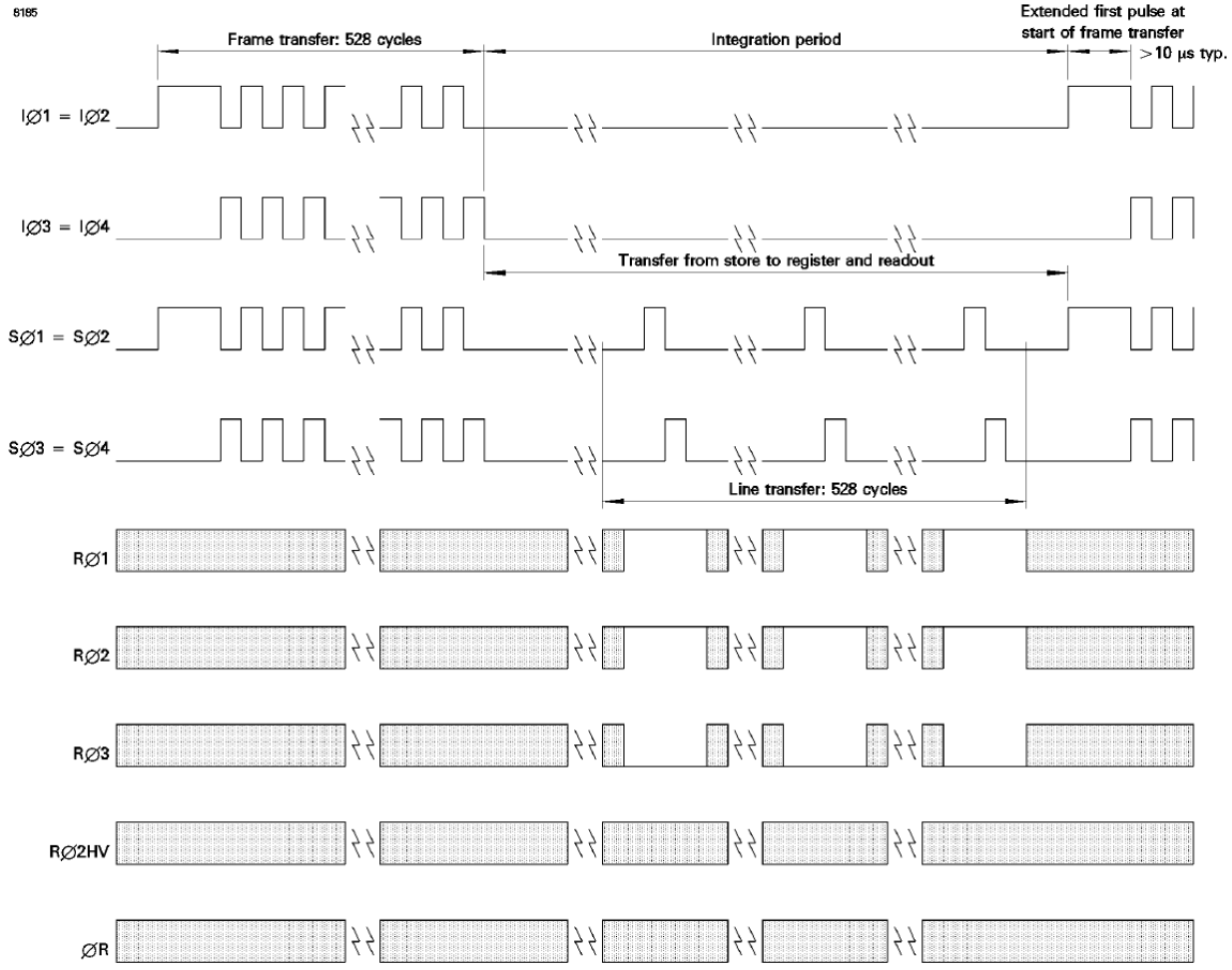


T_W = 10 ns typical
T_1 = output valid
T_2 > 0 ns

Pulse and Output Timing

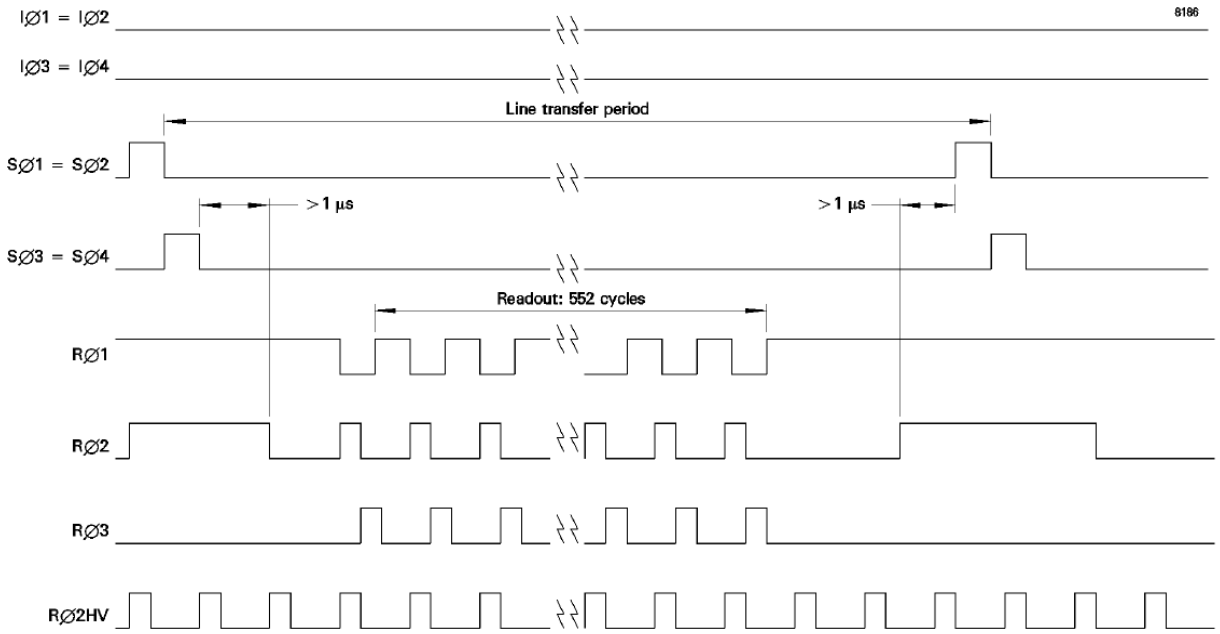


Example Frame Timing Diagram

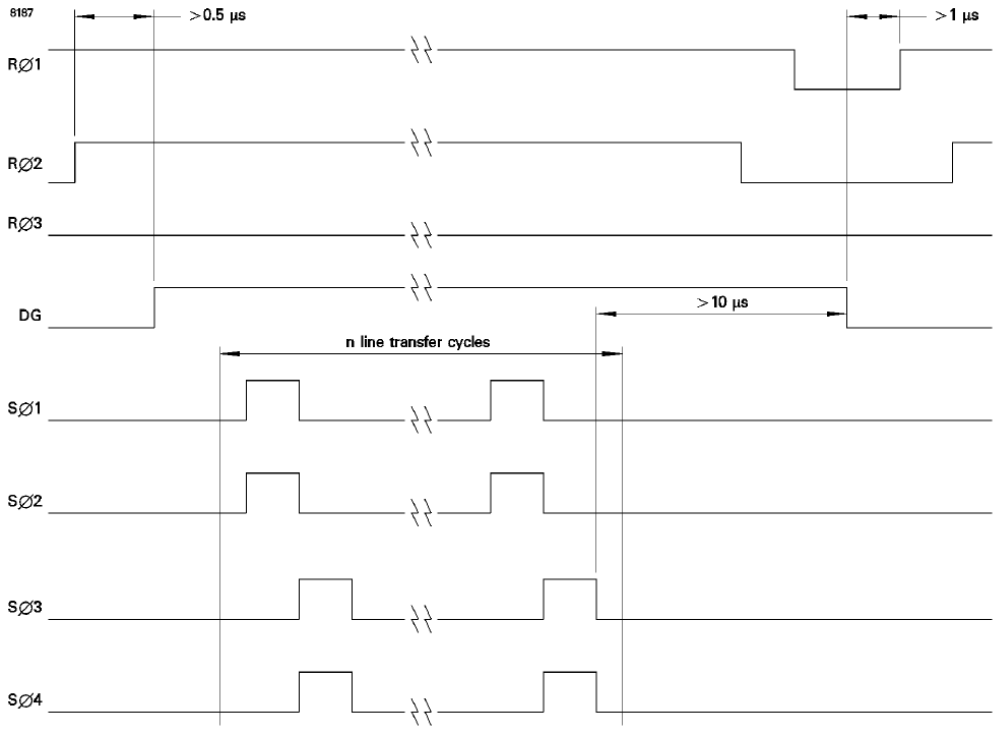


Example Line Timing Diagram

Operation through OSL, see notes 13 and 19



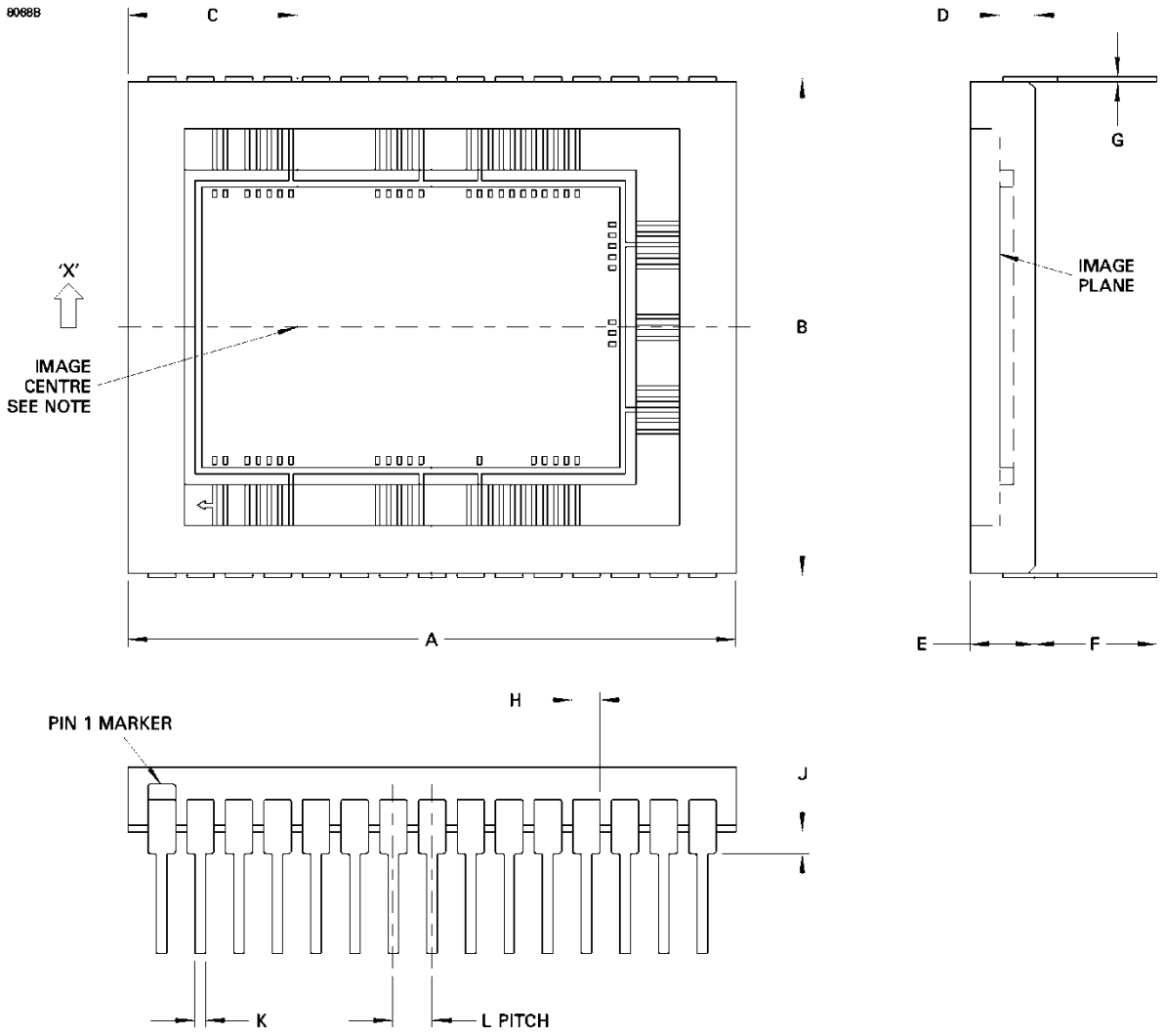
Operation of the Dump Gate to Dump n Lines of Unwanted Data From the Standard Register



Wanted lines of data must be completely read out before dumping unwanted data.

OUTLINE DRAWINGS

PACKAGE OUTLINE (Tolerances are by design and not verified on each part)



The image center is aligned centrally in the package in direction ‘X’, to within a tolerance of ±0.20mm.

HEALTH AND SAFETY HAZARDS

Teledyne e2v devices are safe to handle and operate, provided that the relevant precautions stated herein are observed. Teledyne e2v does not accept responsibility for damage or injury resulting from the use of devices it produces. Equipment manufacturers and users must ensure that adequate precautions are taken. Appropriate warning labels and notices must be provided on equipment incorporating Teledyne e2v devices and in operating manuals.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to an ionising radiation. Users planning to use CCDs in a high radiation environment are advised to contact Teledyne e2v.

TEMPERATURE LIMITS

	Min	Typical	Max
Storage	-200°C		+100°C
Operating	-120°C		+75°C

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling..... 5 K/min

PART REFERENCES

Variant	Operating Mode	Illumination	Enhanced BSI Process	Silicon	AR Coating	Fringe Suppression	Notes
CCD97-00-G-095	2-Phase	BSI	No	Standard	Midband	No	
CCD97-00-G-103	2-Phase	BSI	No	Standard	Midband	No	20
CCD97-00-G-162	2-Phase	BSI	No	Standard	Broadband	No	
CCD97-00-G-172	2-Phase	BSI	No	Standard	Midband	Yes	
CCD97-00-G-175	2-Phase	BSI	No	Standard	Multi-2	No	
CCD97-00-G-177	2-Phase	BSI	No	Standard	UV	No	
CCD97-00-G-180	2-Phase	BSI	No	Standard	Multi-2	Yes	
CCD97-00-G-S28	2-Phase	BSI	No	Standard	Midband	No	21
CCD97-00-G-S74	2-Phase	BSI	Yes	Standard	Multi-19	No	

Grade Definitions

Grade 1	Science Grade	Meets all performance parameters and Grade 1 cosmetic parameters
Grade 5	Engineering Grade	Electrically functional with no performance or cosmetic parameter guarantees
Grade 6	Mechanical Grade	Non-functional. Mechanically representative only.

NOTES

20. Lumogen coated device.
21. OSH output capability not included.
22. G = Grade (e.g. 1)
23. Additional variants may be available to custom order. Consult Teledyne e2v for more information.